QM3816N6

Dual N-Channel Fast Switching MOSFET

General Description

The QM3816N6 is the highest performance trench Dual N-channel MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The QM3816N6 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available

Product Summary

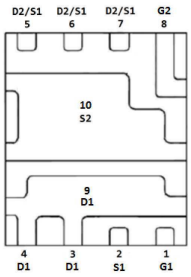
Green RoHS、HF、Pb

	BVDSS	RDSON (VGS=10V)	ID (T_C=25℃)
Die1	30V	7.3mΩ	51A
Die2	30V	1.9mΩ	117A

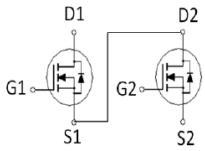
Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- CCFL Back-light Inverter

DFN 5X6 Pin Configuration



Bottom view



Absolute Maximum Ratings(T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Rating		Units
		Die1	Die2	
V_{DS}	Drain-Source Voltage	30	30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	51	117	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	32	74	A
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	13	28	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	10	22	A
I_{DM}	Pulsed Drain Current[2]	102	234	A
EAS	Single Pulse Avalanche Energy[3]	59.5	519.2	mJ
I_{AS}	Avalanche Current	34.5	101.9	A
P_D@T_C=25℃	Total Power Dissipation[4]	31	40	W
P_D@T_A=25℃	Total Power Dissipation[4]	2	2	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	℃

Thermal Data

Symbol	Parameter	Die 1	Die 2	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	62	56	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	4	3.1	℃/W

Die1 N-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.03	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=30A	---	5.8	7.3	mΩ
		V_{GS}=4.5V , I_D=15A	---	9.0	11.7	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.2	---	2.5	V
$\triangle V_{GS(th)}/\triangle T_J$	$V_{GS(th)}$ Temperature Coefficient		---	-5.5	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V , V_{GS}=0V	---	---	1	uA
		V_{DS}=24V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=30A	---	31	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.2	---	Ω
Q_g	Total Gate Charge (10V)	V_{DS}=15V , V_{GS}=10V , I_D=15A	---	18.3	---	nC
Q_g	Total Gate Charge (4.5V)	V_{DS}=15V , V_{GS}=4.5V , I_D=15A	---	9.1	---	nC
Q_{gs}	Gate-Source Charge		---	3.7	---	
Q_{gd}	Gate-Drain Charge		---	3.6	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=3.3Ω I_D=15A	---	7.7	---	ns
T_r	Rise Time		---	37.7	---	
$T_{d(off)}$	Turn-Off Delay Time		---	22.4	---	
T_f	Fall Time		---	9.8	---	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	1022	---	pF
C_{oss}	Output Capacitance		---	160	---	
C_{rss}	Reverse Transfer Capacitance		---	106	---	

Guaranteed Avalanche Characteristics(T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=25V , L=0.1mH , I_{AS}=24A	28.8	---	---	mJ

Diode Characteristics(T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,6]	V_G=V_D=0V , Force Current	---	---	51	A
I_{SM}	Pulsed Source Current[2,6]		---	---	102	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A	---	---	1.2	V

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH.
4.The power dissipation is limited by 150℃ junction temperature
5.The Min. value is 100% EAS tested guarantee.
6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Die2 N-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.03	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=30A	---	1.5	1.9	mΩ
		V_{GS}=4.5V , I_D=15A	---	2.2	2.9	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.2	---	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	6.0	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V , V_{GS}=0V	---	---	1	uA
		V_{DS}=24V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=30A	---	115	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	0.7	---	Ω
Q_g	Total Gate Charge (10V)	V_{DS}=15V , V_{GS}=10V , I_D=15A	---	80.7	---	nC
Q_g	Total Gate Charge (4.5V)	V_{DS}=15V , V_{GS}=4.5V , I_D=15A	---	40.7	---	nC
Q_{gs}	Gate-Source Charge		---	14.7	---	
Q_{gd}	Gate-Drain Charge		---	16.2	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=15V , V_{GS}=10V , R_G=3.3Ω I_D=15A	---	19.1	---	ns
T_r	Rise Time		---	51.6	---	
$T_{d(off)}$	Turn-Off Delay Time		---	68.6	---	
T_f	Fall Time		---	22.5	---	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	4982	---	pF
C_{oss}	Output Capacitance		---	763	---	
C_{rss}	Reverse Transfer Capacitance		---	468	---	

Guaranteed Avalanche Characteristics(T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=25V , L=0.1mH , I_{AS}=72A	259.2	---	---	mJ

Diode Characteristics(T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,6]	V_G=V_D=0V , Force Current	---	---	117	A
I_{SM}	Pulsed Source Current[2,6]		---	---	234	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A	---	---	1.2	V

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=50V,V_{GS}=10V,L=0.1mH.
4.The power dissipation is limited by 150℃ junction temperature
5.The Min. value is 100% EAS tested guarantee.
6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Die 1 Typical Characteristics

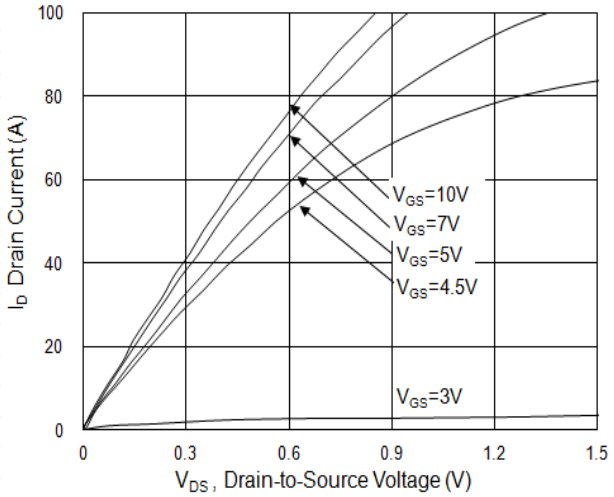


Fig.1 Typical Output Characteristics

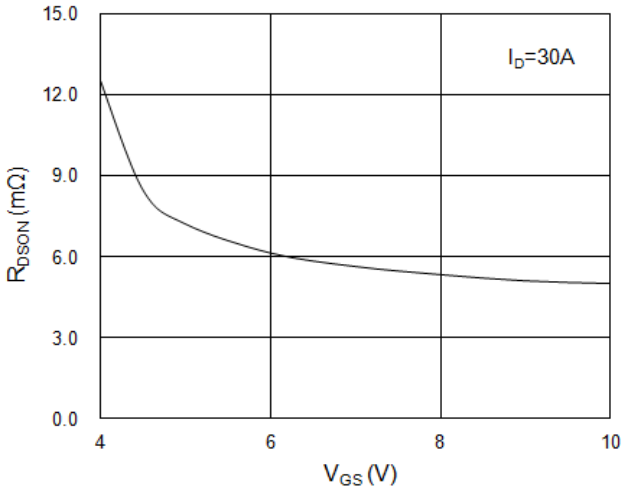


Fig.2 On-Resistance vs. Gate-Source

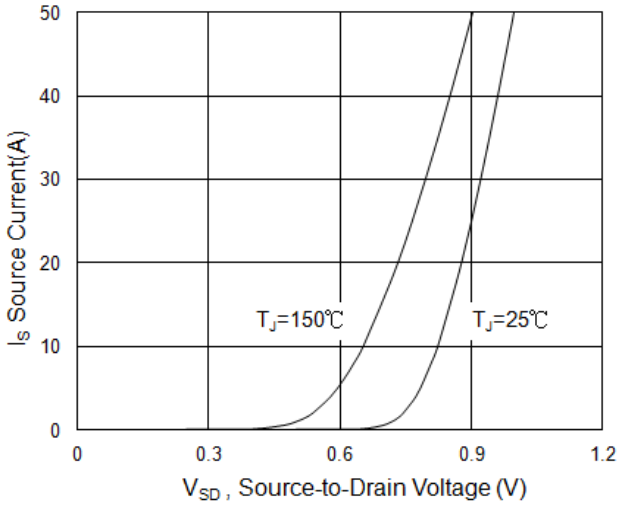


Fig.3 Forward Characteristics of Reverse

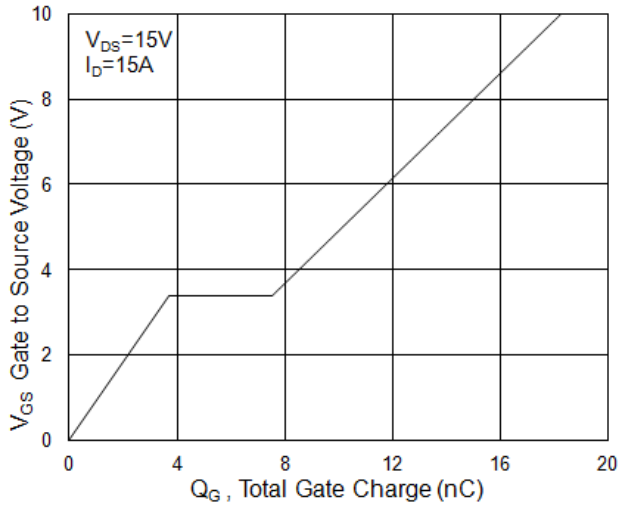


Fig.4 Gate-Charge Characteristics

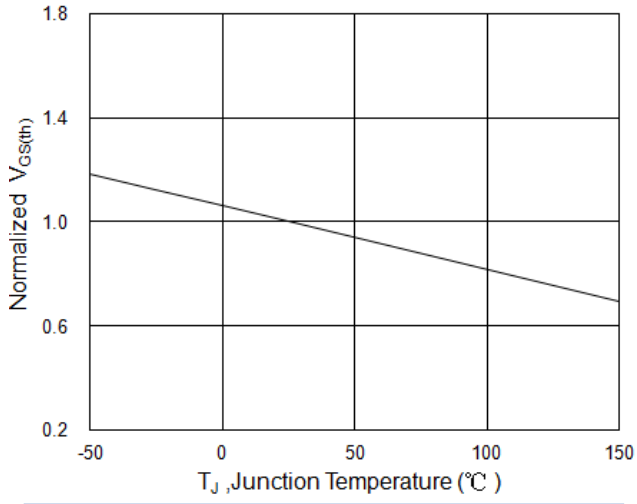


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

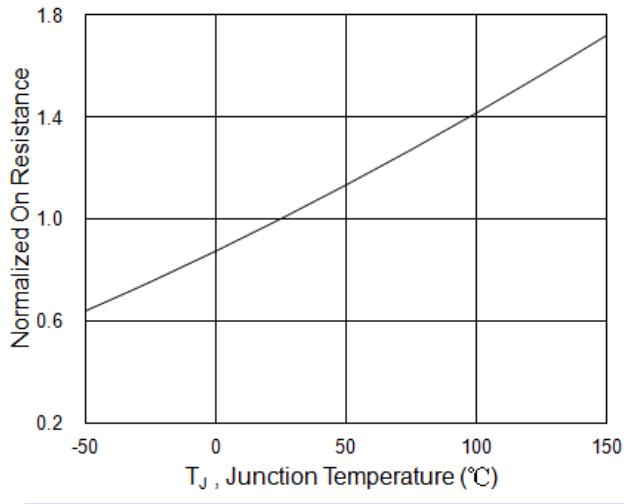


Fig.6 Normalized R_{DSON} vs. T_J

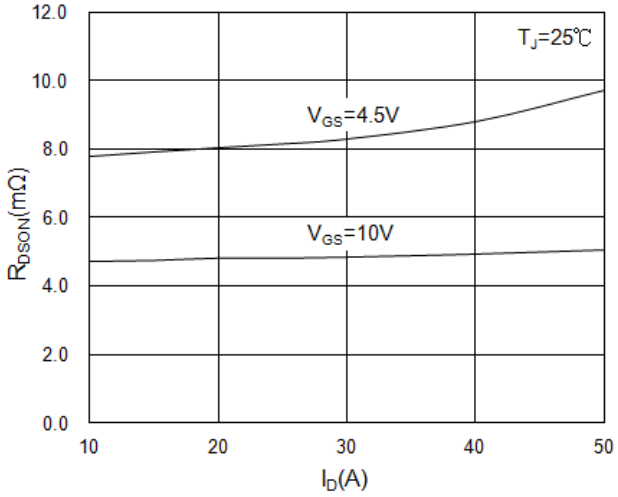


Fig.7 Drain-Source On-State Resistance

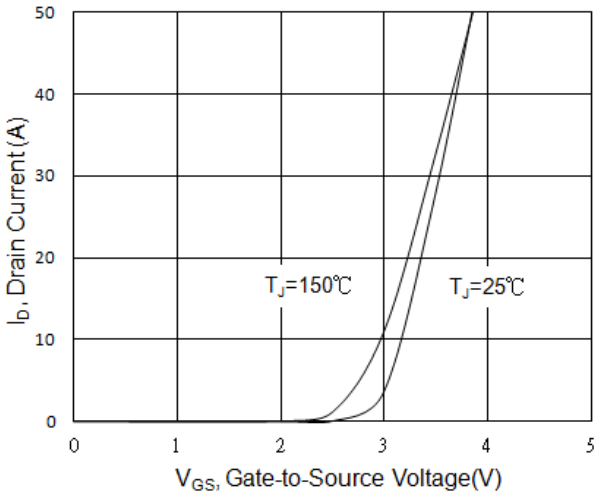


Fig.8 Transfer Characteristics

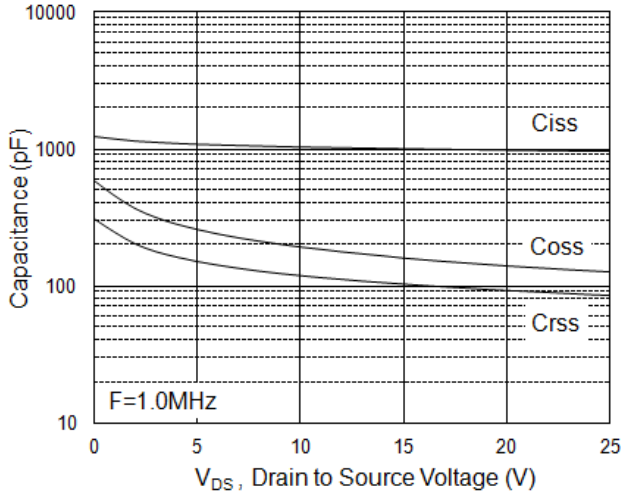


Fig.9 Capacitance

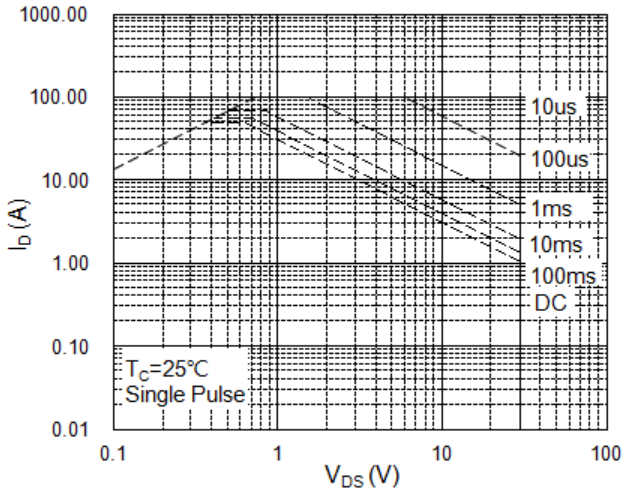


Fig.10 Safe Operating Area

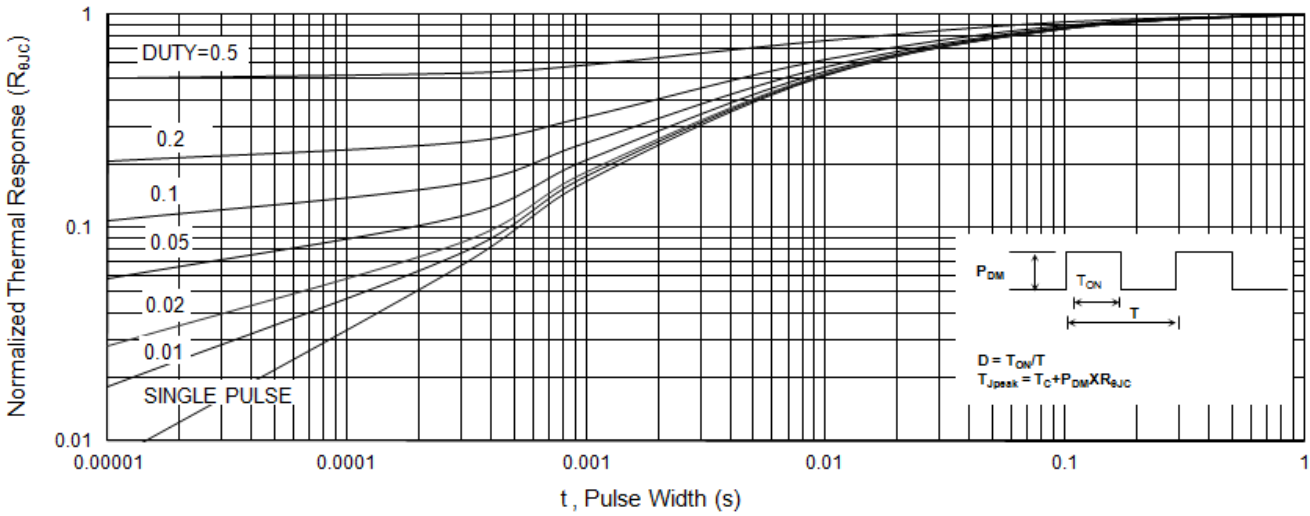


Fig.11 Normalized Maximum Transient Thermal Impedance

Die 2 Typical Characteristics

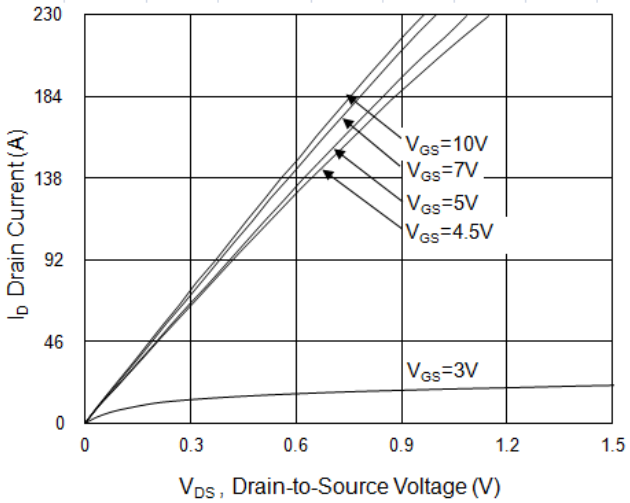


Fig.1 Typical Output Characteristics

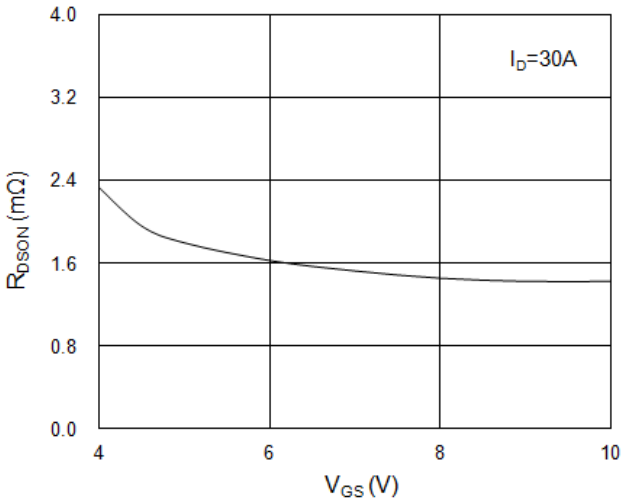


Fig.2 On-Resistance vs. Gate-Source

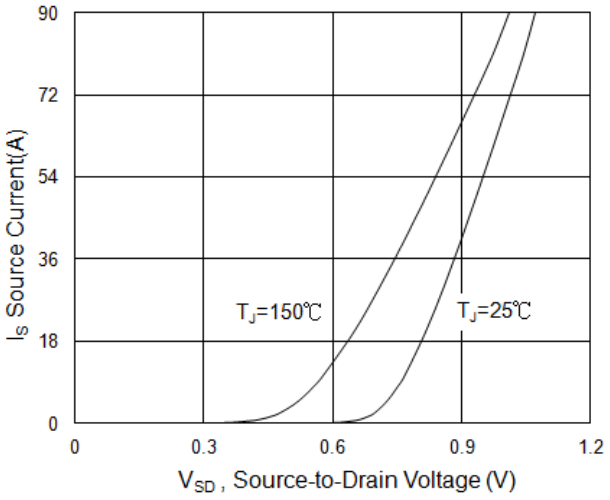


Fig.3 Forward Characteristics of Reverse

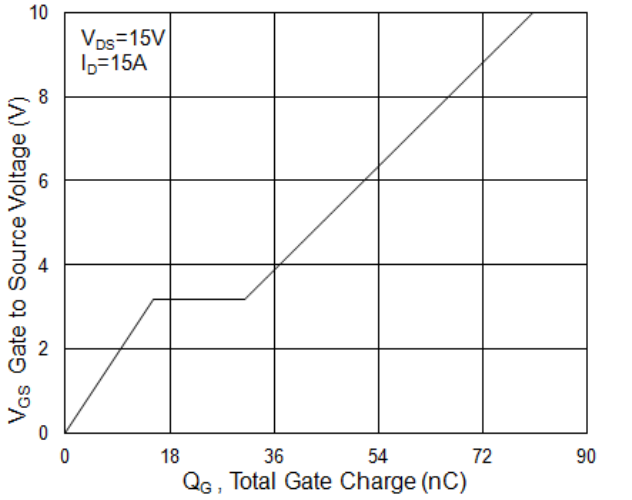


Fig.4 Gate-Charge Characteristics

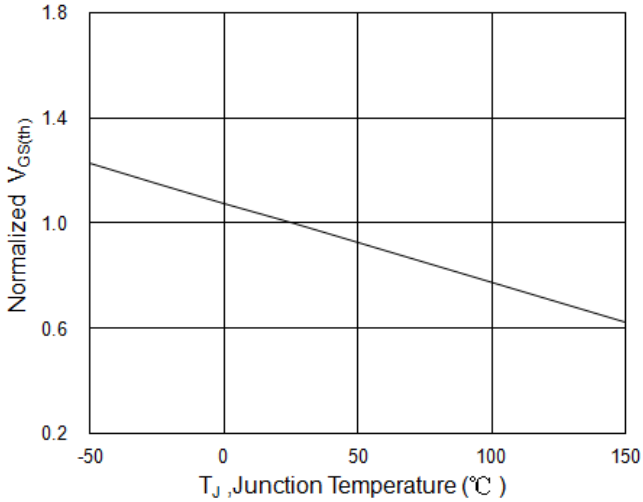


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

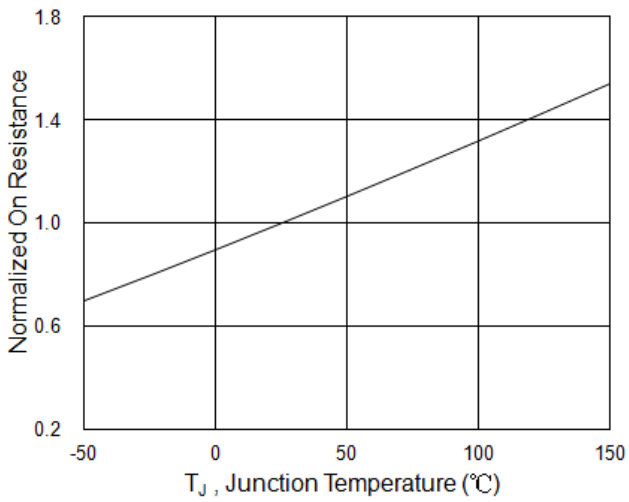


Fig.6 Normalized R_{DSON} vs. T_J

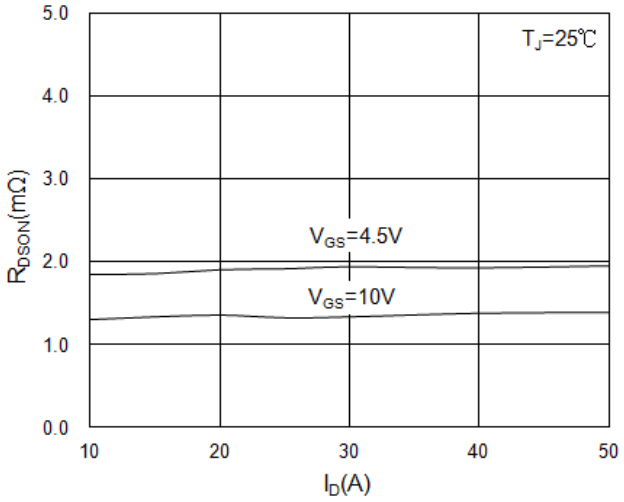


Fig.7 Drain-Source On-State Resistance

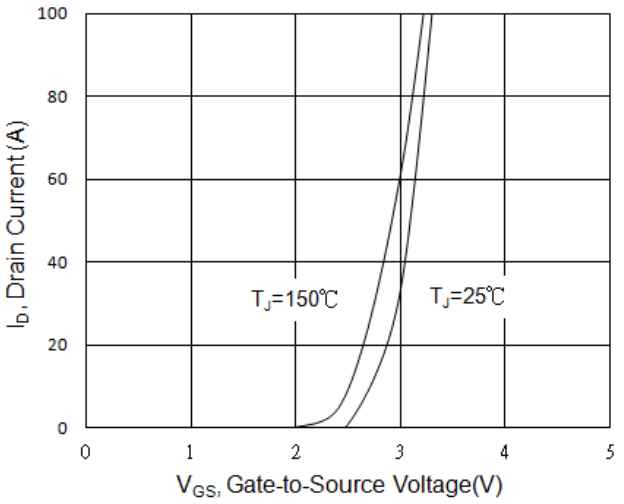


Fig.8 Transfer Characteristics

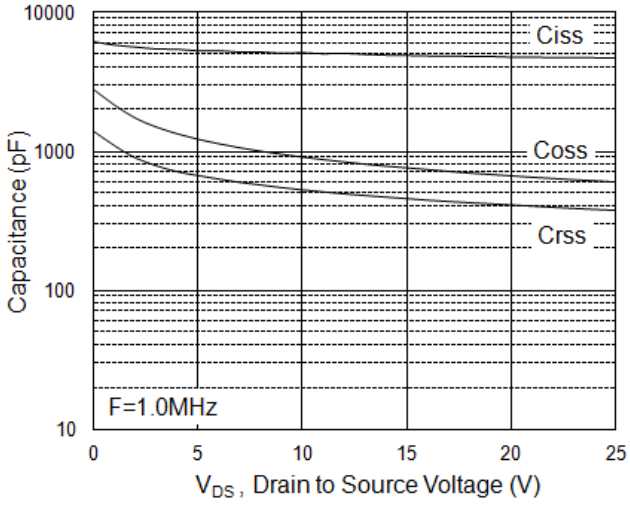


Fig.9 Capacitance

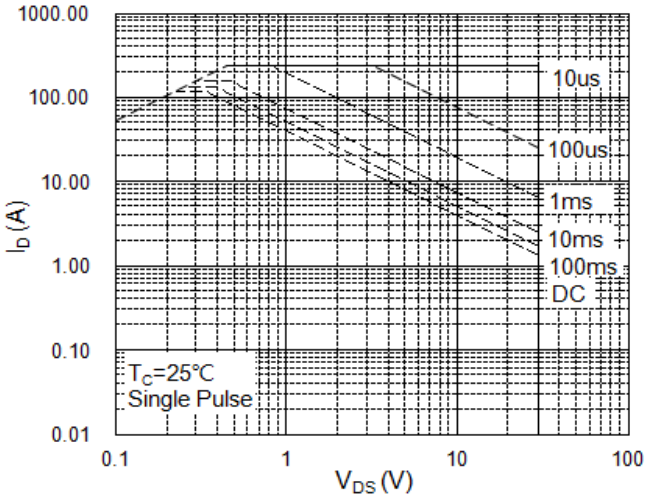


Fig.10 Safe Operating Area

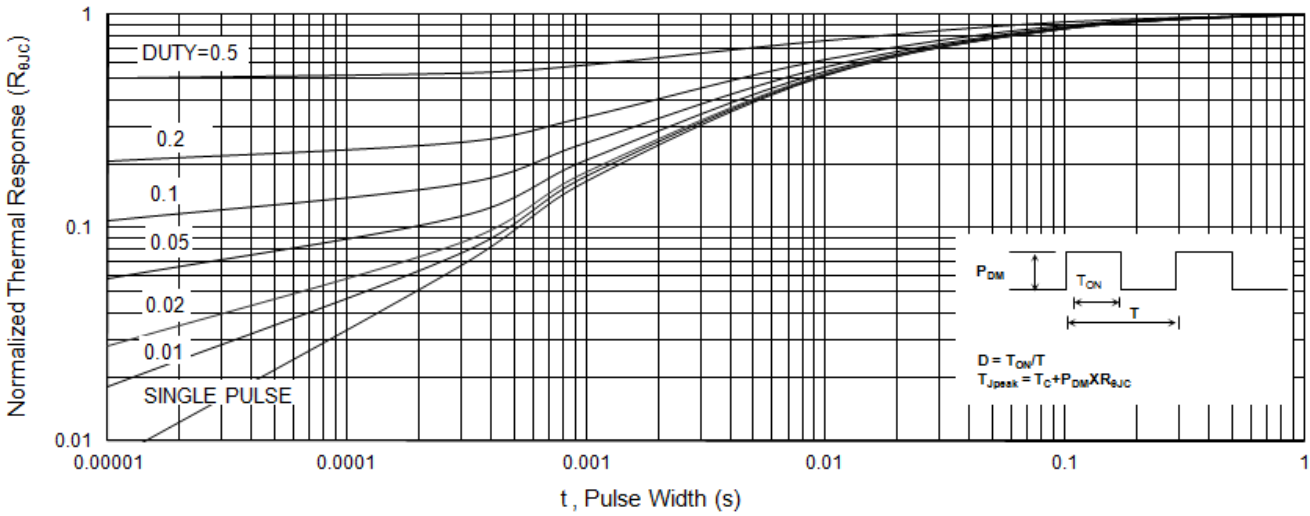
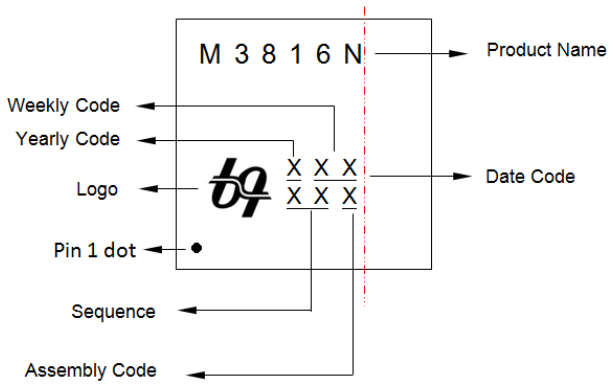
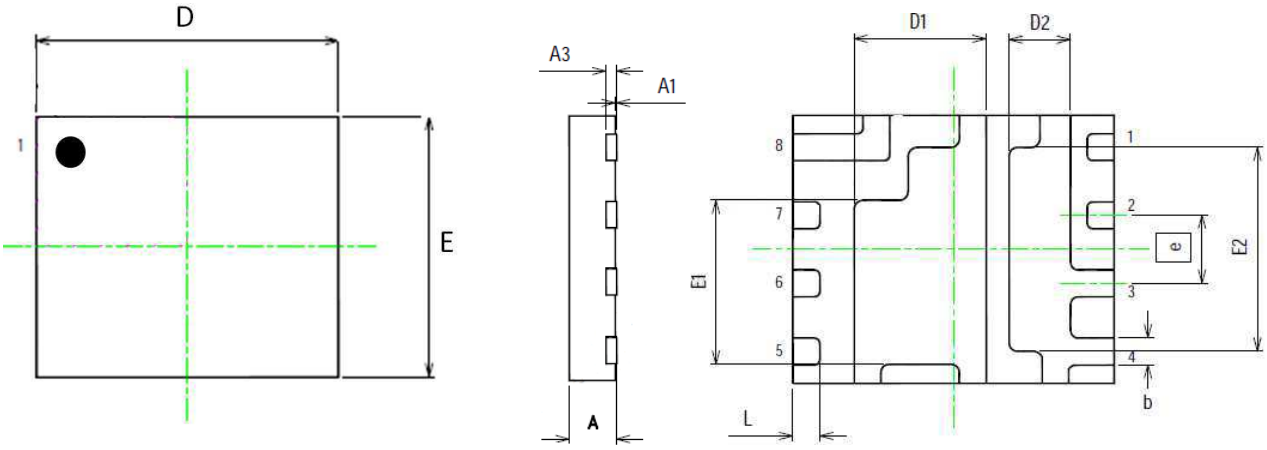


Fig.11 Normalized Maximum Transient Thermal Impedance

Top Marking

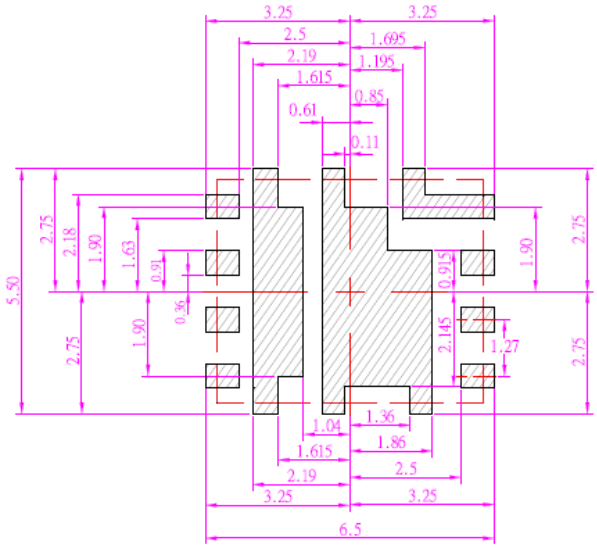


DFN 5X6 Package Outline Drawing



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	--	0.203	--
b	0.40	0.50	0.60
D	--	6.00	--
E	--	5.00	--
e	--	1.27	--
D1	2.37	2.47	2.57
E1	2.96	3.06	3.16
D2	1.05	1.15	1.25
E2	3.70	3.80	3.90
L	0.40	0.50	0.60

Note:
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.



LAND PATTERN RECOMMENDATION (Unit :mm)