



FDPC5018SG

PowerTrench® Power Clip 30V Asymmetric Dual N-Channel MOSFET

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 5.0 mΩ at $V_{GS} = 10$ V, $I_D = 17$ A
- Max $r_{DS(on)}$ = 6.5 mΩ at $V_{GS} = 4.5$ V, $I_D = 14$ A

Q2: N-Channel

- Max $r_{DS(on)}$ = 1.6 mΩ at $V_{GS} = 10$ V, $I_D = 32$ A
- Max $r_{DS(on)}$ = 2.0 mΩ at $V_{GS} = 4.5$ V, $I_D = 28$ A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- RoHS Compliant

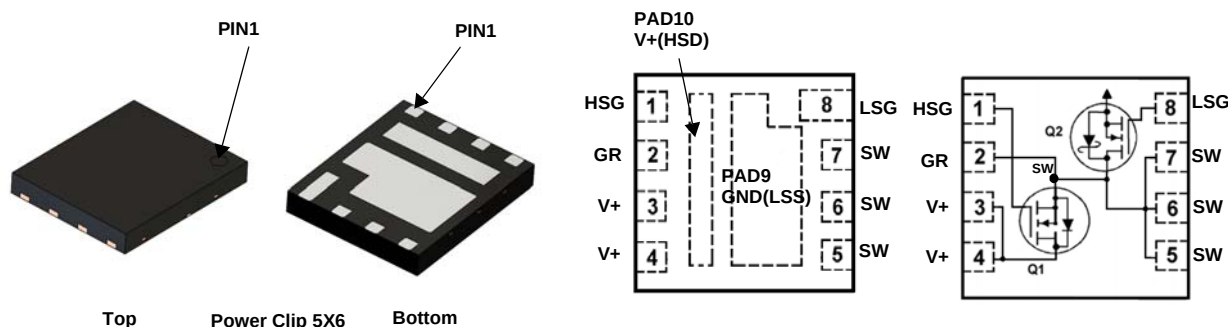


General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load



Pin	Name	Description	Pin	Name	Description	Pin	Name	Description
1	HSG	High Side Gate	3,4,10	V+(HSD)	High Side Drain	8	LSG	Low Side Gate
2	GR	Gate Return	5,6,7	SW	Switching Node, Low Side Drain	9	GND(LSS)	Low Side Source

MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	30	30	V
$Bvdsst$	$Bvdsst$ (transient) < 100nS	32.5	32.5	V
V_{GS}	Gate to Source Voltage	± 20	± 12	V
I_D	Drain Current -Continuous $T_C = 25^\circ\text{C}$ (Note 5)	56	109	A
	-Continuous $T_C = 100^\circ\text{C}$ (Note 5)	35	69	
	-Continuous $T_A = 25^\circ\text{C}$	17 ^{Note1a}	32 ^{Note1b}	
	-Pulsed $T_A = 25^\circ\text{C}$ (Note 4)	227	704	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	54	181	mJ
P_D	Power Dissipation for Single Operation $T_C = 25^\circ\text{C}$	23	29	W
	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	2.1 ^{Note1a}	2.3 ^{Note1b}	
	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	1.0 ^{Note1c}	1.1 ^{Note1d}	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.6	4.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 ^{Note1a}	55 ^{Note1b}	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 ^{Note1c}	120 ^{Note1d}	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDPC5018SG	FDPC5018SG	Power Clip 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$ $I_D = 10\text{ mA}$, referenced to $25\text{ }^{\circ}\text{C}$	Q1 Q2		15 19		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$ $V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$	Q1 Q2			1 500	μA μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$ $V_{GS} = 12\text{ V}$, $V_{DS} = 0\text{ V}$	Q1 Q2			100 100	nA nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$	Q1 Q2	1.0 1.0	1.7 1.6	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$ $I_D = 10\text{ mA}$, referenced to $25\text{ }^{\circ}\text{C}$	Q1 Q2		-5 -3		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 17\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 14\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 17\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$	Q1		4.1 5.4 5.7	5.0 6.5 7.0	m Ω
		$V_{GS} = 10\text{ V}$, $I_D = 32\text{ A}$ $V_{GS} = 4.5\text{ V}$, $I_D = 28\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 32\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$	Q2		1.4 1.7 2.1	1.6 2.0 2.4	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 17\text{ A}$	Q1		93		S
		$V_{DS} = 5\text{ V}$, $I_D = 32\text{ A}$	Q2		188		

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1: Q2:	Q1 Q2		1224 4593	1715 6430	pF
C_{oss}	Output Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	Q1 Q2		397 1210	560 1695	
C_{rss}	Reverse Transfer Capacitance	Q2: $V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	Q1 Q2		42 80	60 115	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	0.5 0.8	1.5 2.4	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = 15\text{ V}$, $I_D = 17\text{ A}$, $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		8 14	16 25	ns
t_r	Rise Time		Q1 Q2		2 5	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2: $V_{DD} = 15\text{ V}$, $I_D = 32\text{ A}$, $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		18 38	33 61	ns
t_f	Fall Time		Q1 Q2		2 4	10 10	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 10 V	Q1 Q2		17 62	24 87	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 4.5 V	Q1 Q2		8 28	11 40	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 15\text{ V}$, $I_D = 17\text{ A}$ $V_{DD} = 15\text{ V}$, $I_D = 32\text{ A}$	Q1 Q2		3.1 11		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2		2.0 5.3		nC

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

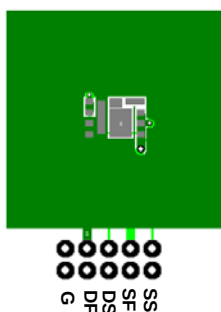
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Drain-Source Diode Characteristics

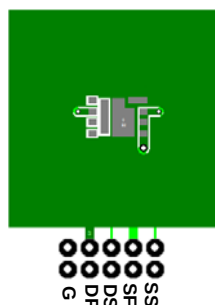
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 17\text{ A}$ (Note 2)	Q1		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 32\text{ A}$ (Note 2)	Q2		0.8	1.2	
t_{rr}	Reverse Recovery Time	Q1 $I_F = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		23	37	ns
			Q2		32	51	
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = 32\text{ A}, di/dt = 240\text{ A}/\mu\text{s}$	Q1		8	16	nC
			Q2		40	64	

Notes:

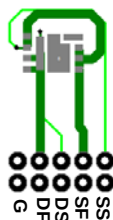
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material, $R_{\theta CA}$ is determined by the user's board design.



a. 60 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 55 °C/W when mounted on a 1 in² pad of 2 oz copper



c. 130 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2 Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Q1 : E_{AS} of 54 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 3\text{ mH}$, $I_{AS} = 6\text{ A}$, $V_{DD} = 30\text{ V}$, $V_{GS} = 10\text{ V}$. 100% tested at $L = 0.1\text{ mH}$, $I_{AS} = 20\text{ A}$.

Q2: E_{AS} of 181 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 3\text{ mH}$, $I_{AS} = 11\text{ A}$, $V_{DD} = 30\text{ V}$, $V_{GS} = 10\text{ V}$. 100% tested at $L = 0.1\text{ mH}$, $I_{AS} = 36\text{ A}$.

4. Pulsed I_d refer to Fig.11 and Fig.24 SOA curve for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

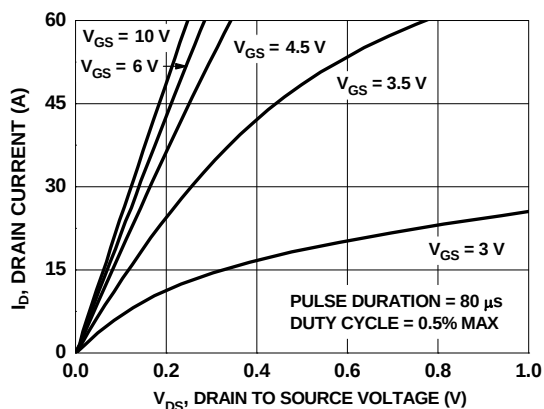


Figure 1. On Region Characteristics

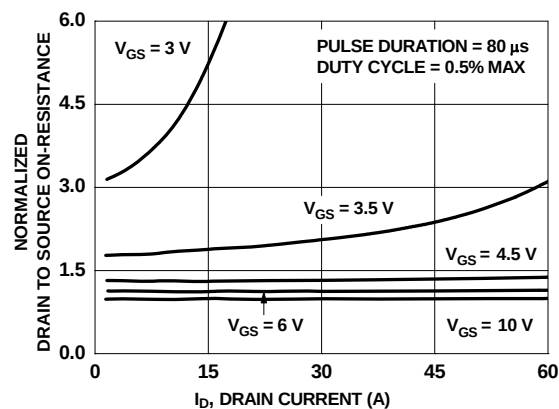


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

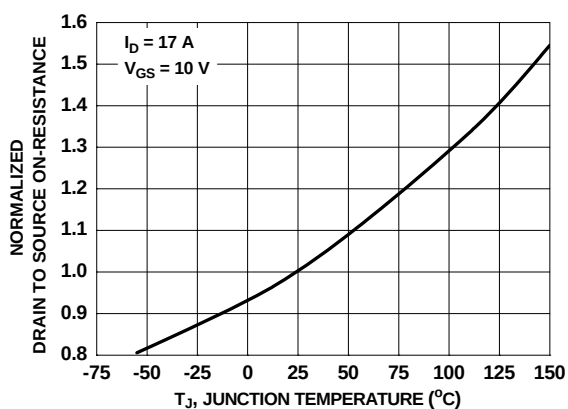


Figure 3. Normalized On Resistance vs. Junction Temperature

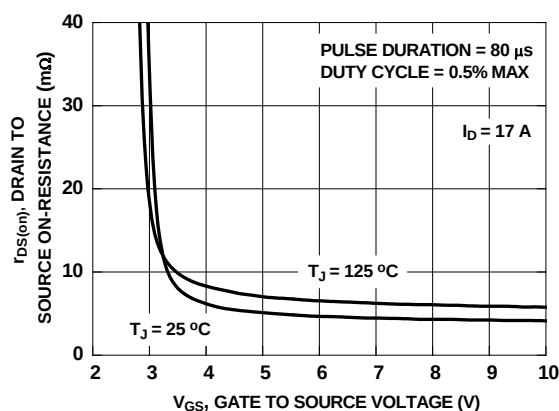


Figure 4. On-Resistance vs. Gate to Source Voltage

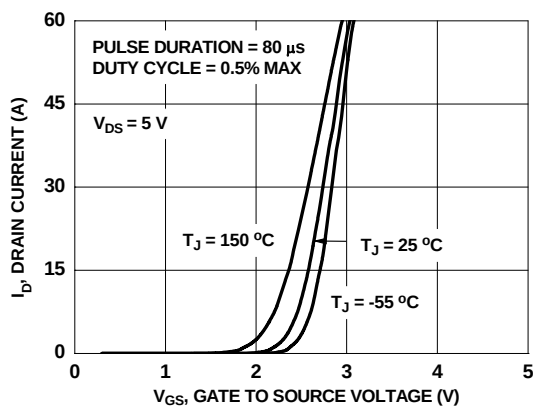


Figure 5. Transfer Characteristics

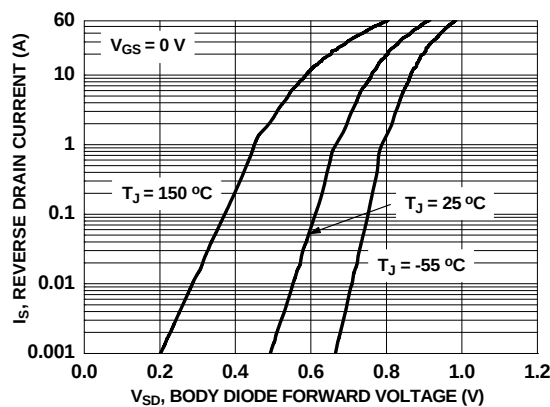


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

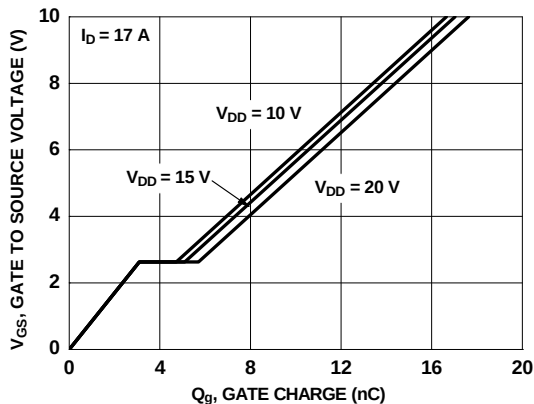


Figure 7. Gate Charge Characteristics

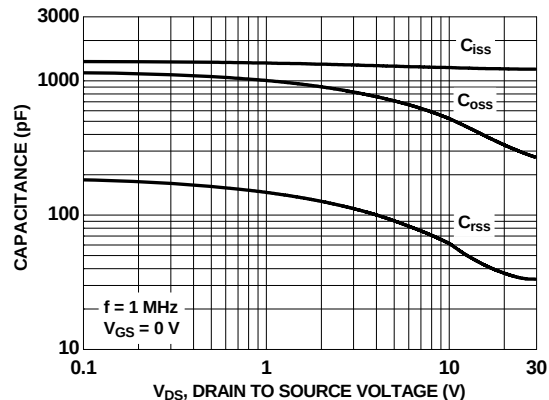


Figure 8. Capacitance vs. Drain to Source Voltage

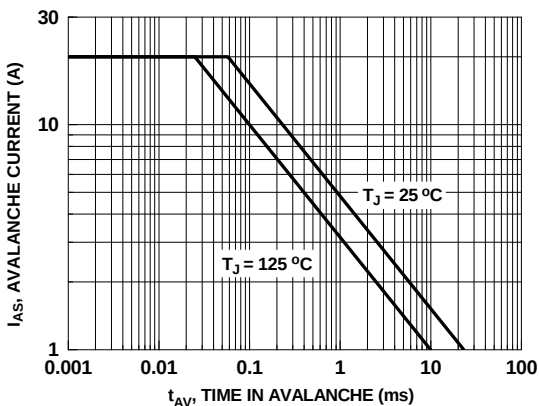


Figure 9. Unclamped Inductive Switching Capability

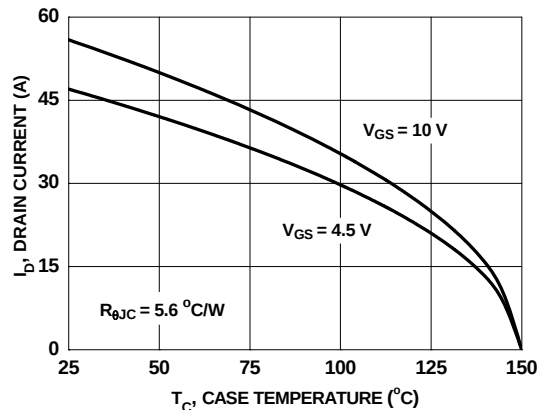


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

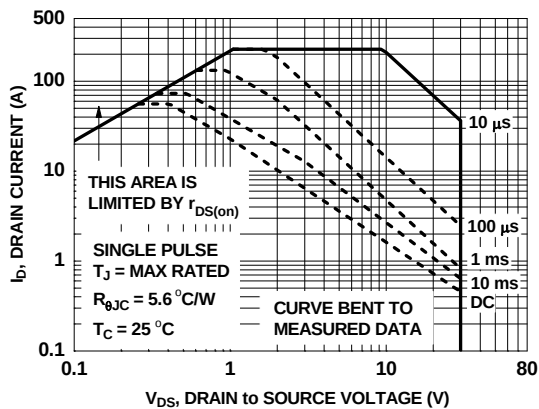


Figure 11. Forward Bias Safe Operating Area

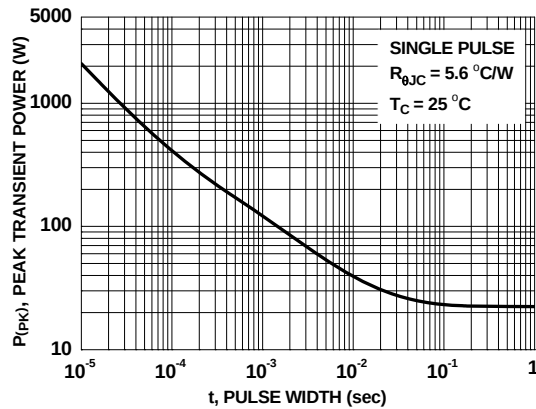


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

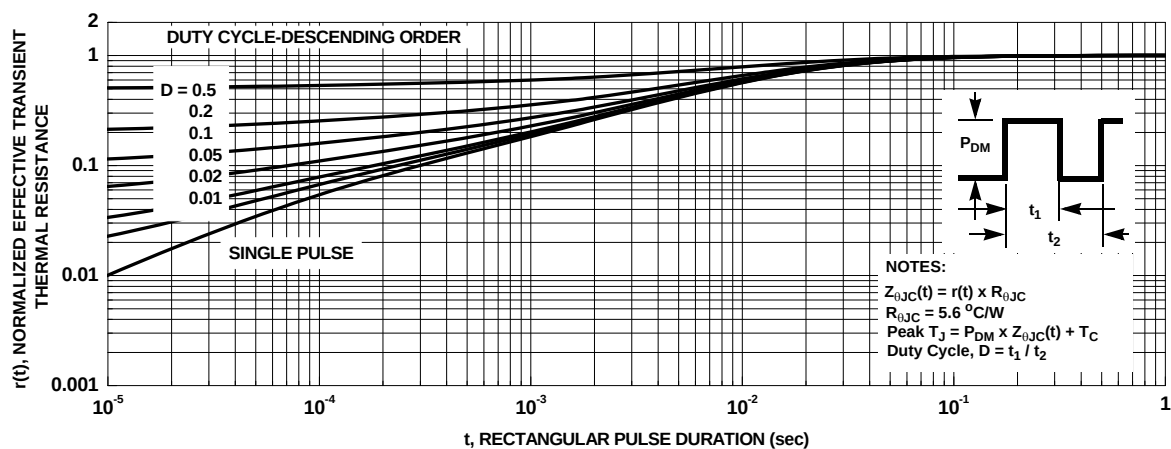


Figure 13. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

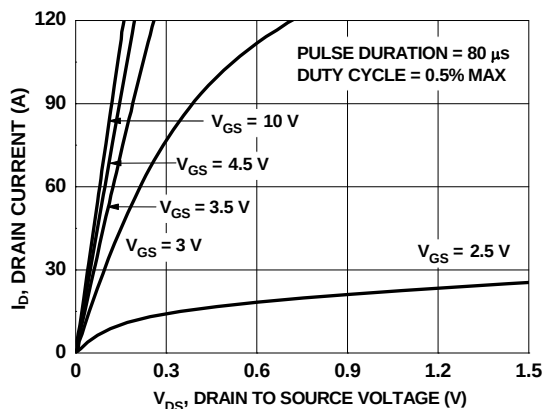


Figure 14. On- Region Characteristics

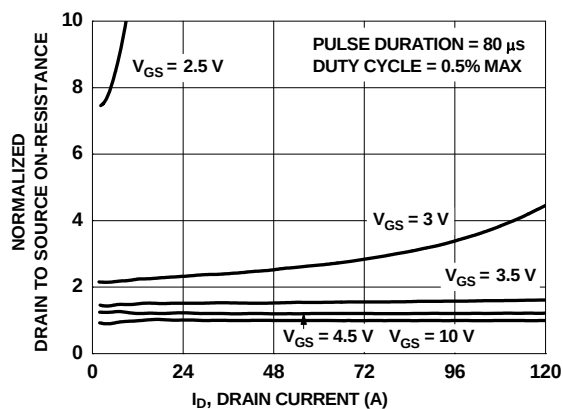


Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage

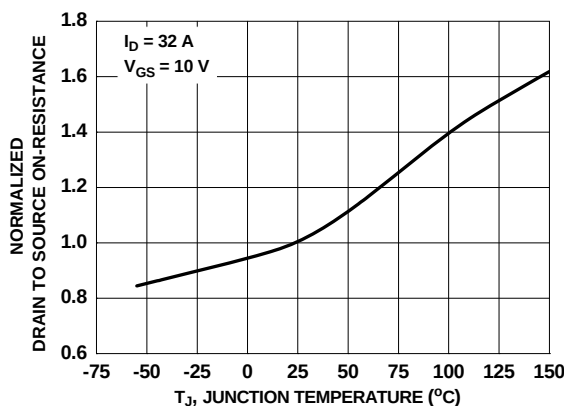


Figure 16. Normalized On-Resistance vs. Junction Temperature

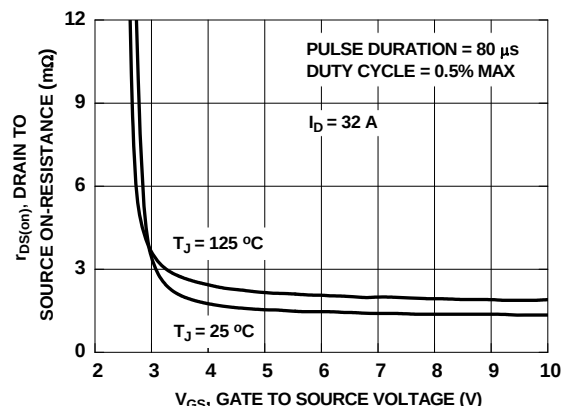


Figure 17. On-Resistance vs. Gate to Source Voltage

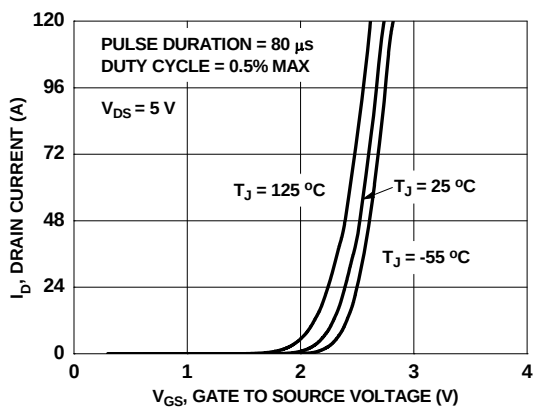


Figure 18. Transfer Characteristics

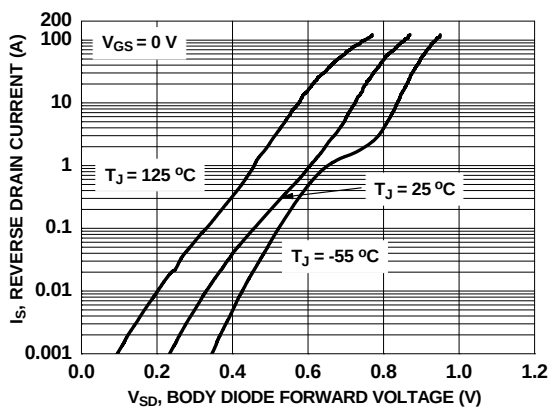


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted.

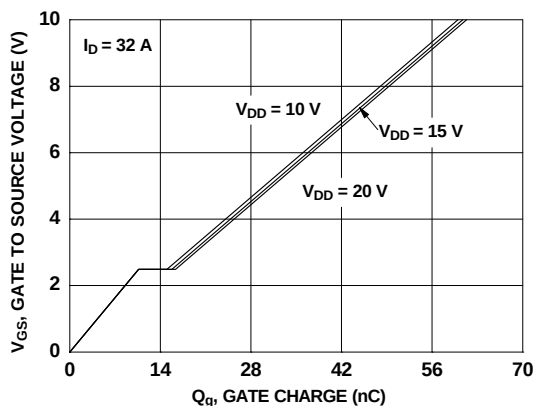


Figure 20. Gate Charge Characteristics

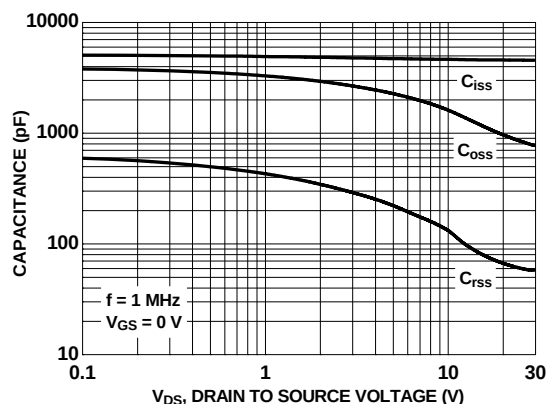


Figure 21. Capacitance vs. Drain to Source Voltage

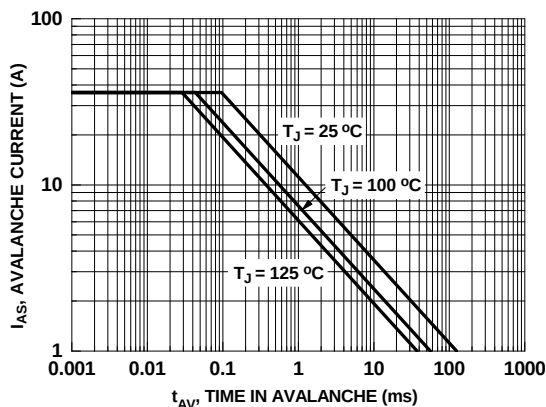


Figure 22. Unclamped Inductive Switching Capability

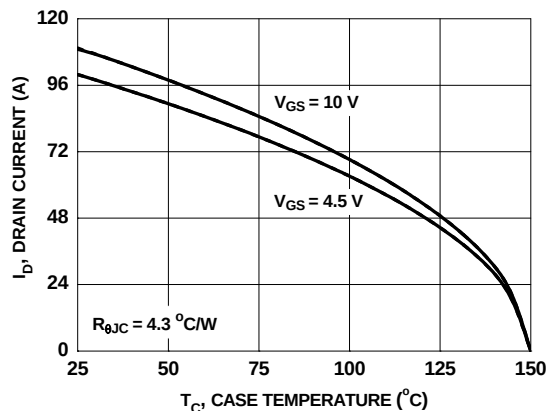


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

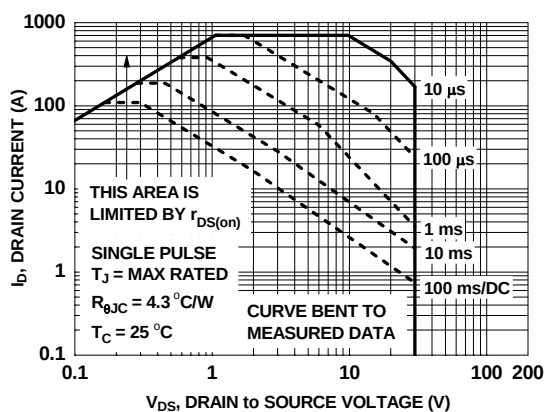


Figure 24. Forward Bias Safe Operating Area

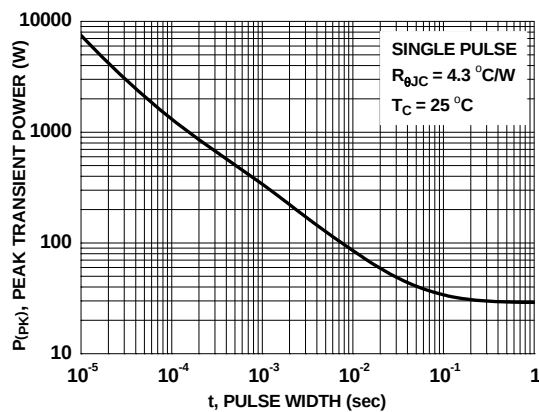


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N-Channel) $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted.

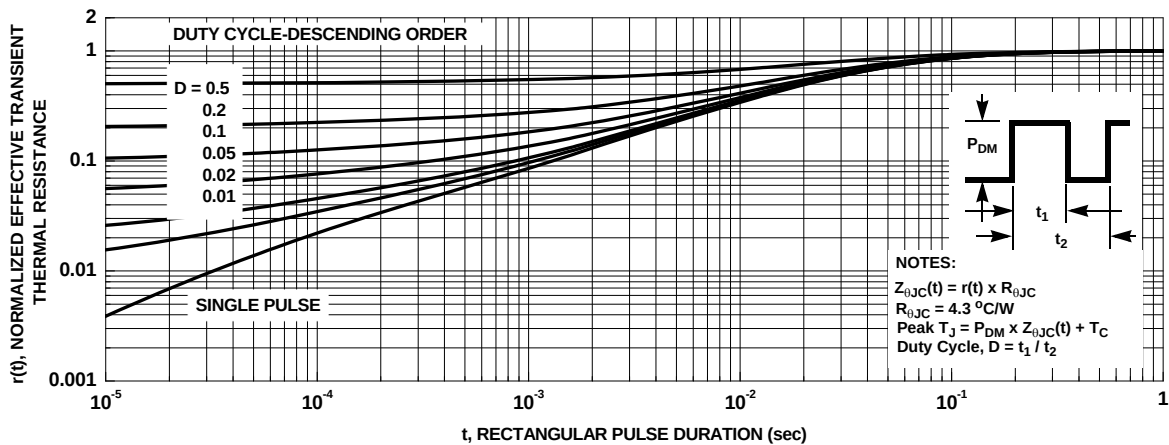


Figure 26. Junction-to-Case Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET™ Schottky Body Diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench® MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC5018SG.

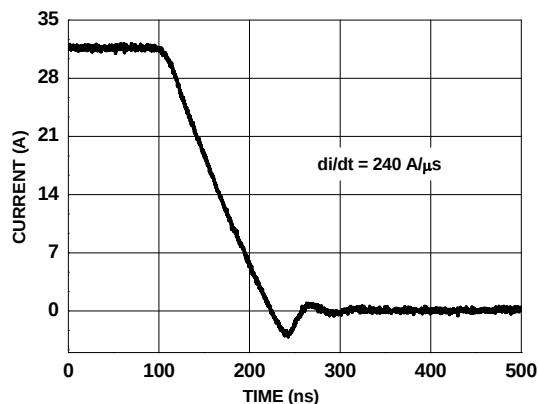


Figure 27. FDPC5018SG SyncFET™ Body Diode Reverse Recovery Characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

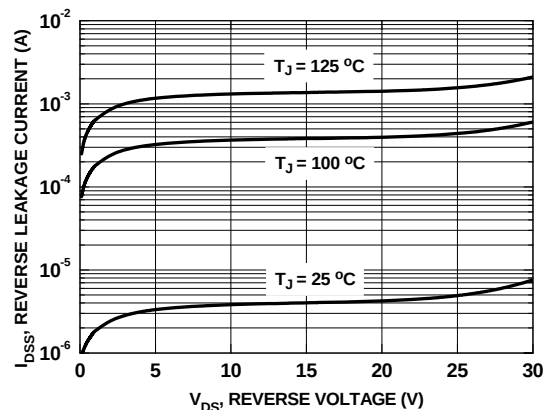
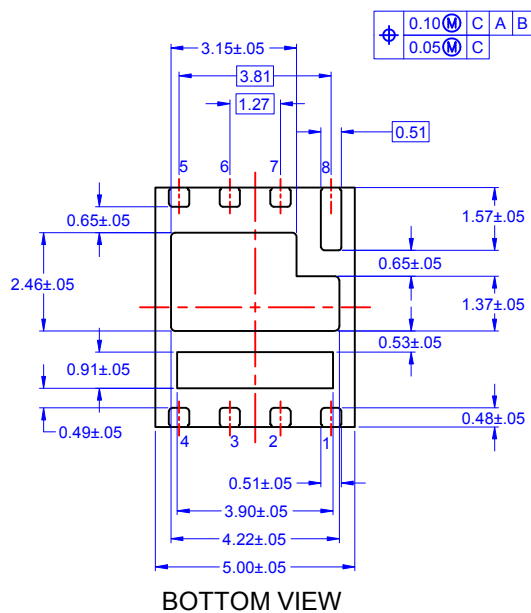
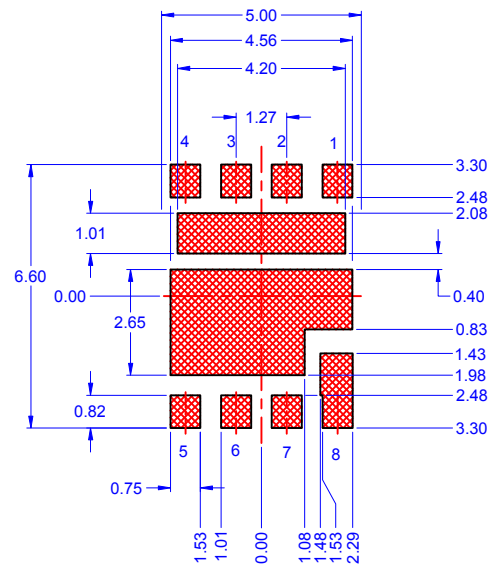
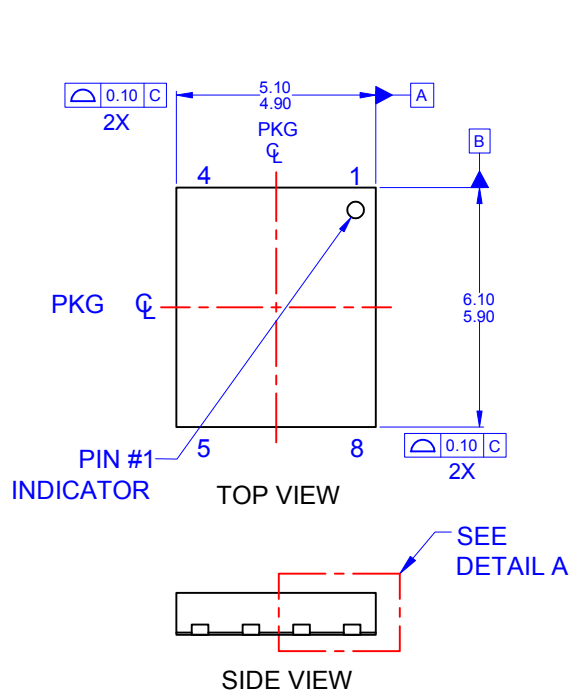
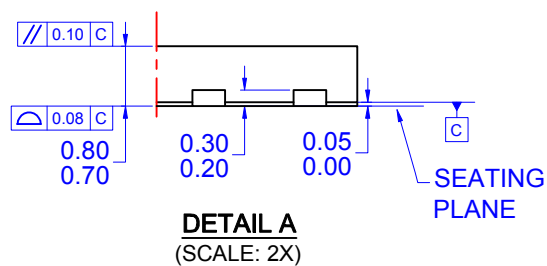


Figure 28. SyncFET™ Body Diode Reverse Leakage vs. Drain-Source Voltage



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) DRAWING FILE NAME: PQFN08KREV2



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