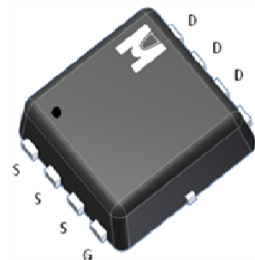
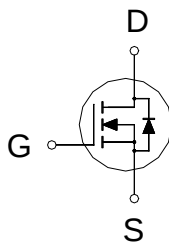


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	30V
$R_{DS(on)} (MAX.)$	11.5m Ω
I_D	18.5A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	18.5	A
	$T_C = 100\text{ }^{\circ}\text{C}$		13.5	
Pulsed Drain Current ¹		I_{DM}	74	
Avalanche Current		I_{AS}	12	
Avalanche Energy	$L = 0.1\text{mH}, I_D = 12\text{A}, R_G = 25\text{ }\Omega$	E_{AS}	7.2	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	3.6	
Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	21	W
	$T_C = 100\text{ }^{\circ}\text{C}$		8.3	
Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$	P_D	2.5	W
	$T_A = 100\text{ }^{\circ}\text{C}$		1	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	$^{\circ}\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³50 $^{\circ}\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.7	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125\text{ }^{\circ}C$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	18.5			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 12A$		9.7	11.5	m Ω
		$V_{GS} = 4.5V, I_D = 7A$		13	16	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 12A$		15		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		1050		pF
Output Capacitance	C_{oss}			141		
Reverse Transfer Capacitance	C_{rss}			87		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		1.2		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=10V)$	$V_{DS} = 15V, V_{GS} = 10V,$ $I_D = 12A$		17.6		nC
	$Q_g(V_{GS}=4.5V)$			9.0		
Gate-Source Charge ^{1,2}	Q_{gs}			2.6		
Gate-Drain Charge ^{1,2}	Q_{gd}			4.0		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 15V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 2.7\Omega$		8		nS
Rise Time ^{1,2}	t_r			8		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			15		
Fall Time ^{1,2}	t_f			10		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _C = 25 °C)						
Continuous Current	I_S				2.5	A
Pulsed Current ³	I_{SM}				10	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.2	V
Reverse Recovery Time	t_{rr}	$I_F = I_S, dI_F/dt = 100A / \mu S$		18		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			40		A
Reverse Recovery Charge	Q_{rr}			10		nC

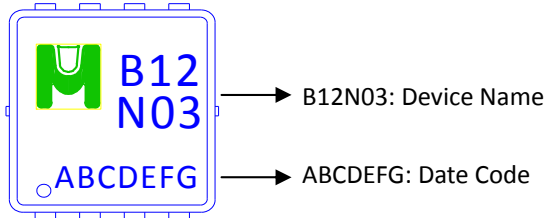
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

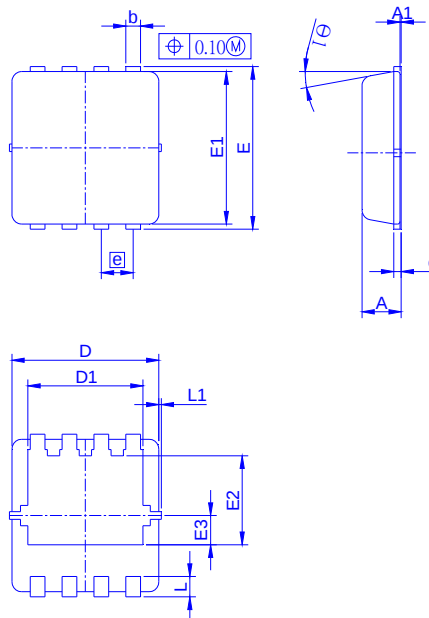
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB12N03V for EDFN 3 x 3



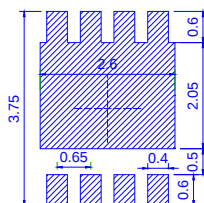
Outline Drawing



Dimension in mm

Dimension	A	A1	b	c	D	D1	E	E1	E2	E3	e	L	L1	$\theta 1$
Min.	0.70	0	0.24	0.10	2.95	2.25	3.15	2.95	1.65			0.30		0°
Typ.	0.80		0.30	0.152	3.00	2.35	3.20	3.00	1.75	0.575	0.65	0.40	0.13	10°
Max.	0.90	0.05	0.37	0.25	3.15	2.45	3.40	3.15	1.96			0.50		12°

Recommended minimum pads





TYPICAL CHARACTERISTICS

