



**Advanced Power
Electronics Corp.**

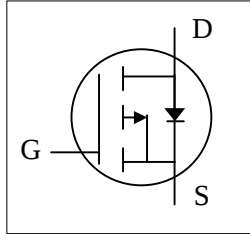
AP3P3R0MT

Halogen-Free Product

P-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Ultra Low On-resistance
- ▼ RoHS Compliant & Halogen-Free

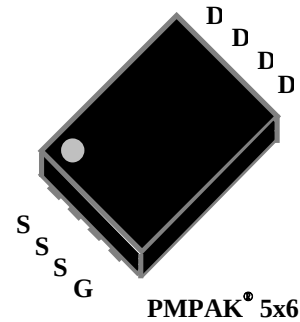


BV _{DSS}	-30V
R _{DS(ON)}	3mΩ
I _D ⁴	-125A

Description

AP3P3R0 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 5x6 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.



Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	-30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Drain Current (Chip), V _{GS} @ 10V ⁴	-125	A
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴ (Package Limited)	-60	A
I _D @T _A =25°C	Drain Current ³ , V _{GS} @ 10V	-33.5	A
I _D @T _A =70°C	Drain Current ³ , V _{GS} @ 10V	-26.8	A
I _{DM}	Pulsed Drain Current ¹	-200	A
P _D @T _C =25°C	Total Power Dissipation	69.4	W
P _D @T _A =25°C	Total Power Dissipation	5	W
E _{AS}	Single Pulse Avalanche Energy ⁵	45	mJ
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Unit
R _{thj-c}	Maximum Thermal Resistance, Junction-case	1.8	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	25	°C/W



AP3P3R0MT

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-20A	-	-	3	mΩ
		V _{GS} =-4.5V, I _D =-10A	-	-	4.5	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-	-3	V
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-20A	-	67	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V	-	-	-10	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =-20A	-	76	122	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-15V	-	24	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-4.5V	-	26	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =-15V	-	19	-	ns
t _r	Rise Time	I _D =-1A	-	12	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	160	-	ns
t _f	Fall Time	V _{GS} =-10V	-	74	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	9400	15040	pF
C _{oss}	Output Capacitance	V _{DS} =-15V	-	1230	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	680	-	pF
R _g	Gate Resistance	f=1.0MHz	-	3	6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =-20A, V _{GS} =0V	-	-	-1.2	V
t _{rr}	Reverse Recovery Time	I _S =-20A, V _{GS} =0V,	-	36	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	30	-	nC

Notes:

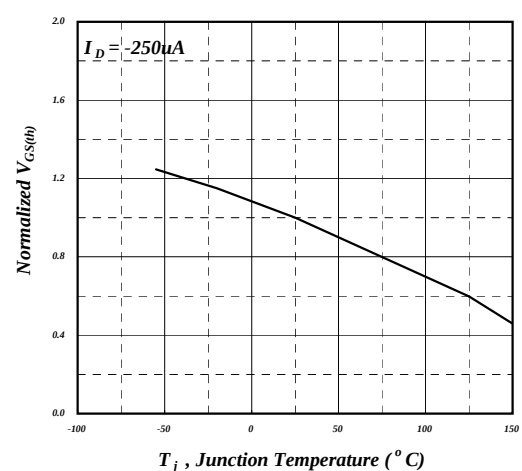
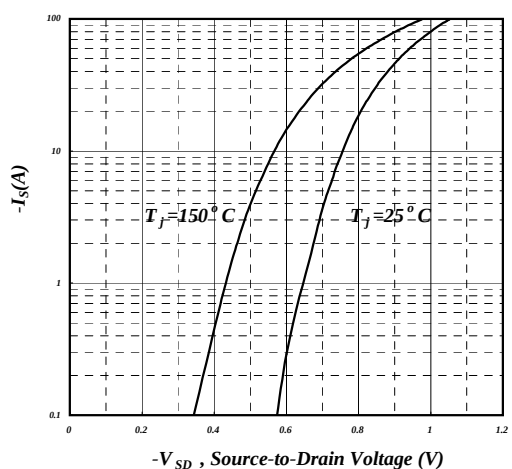
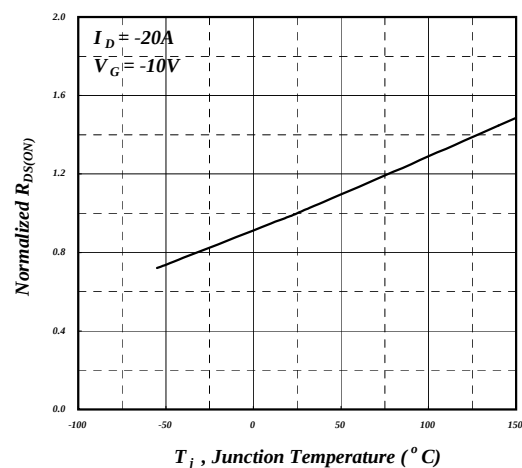
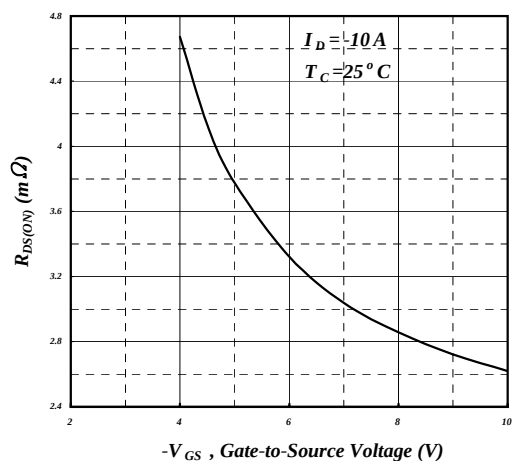
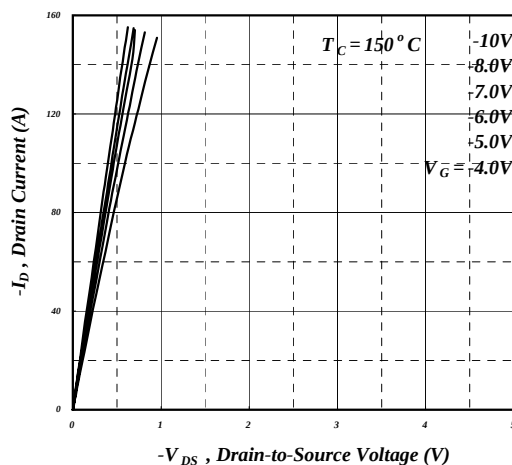
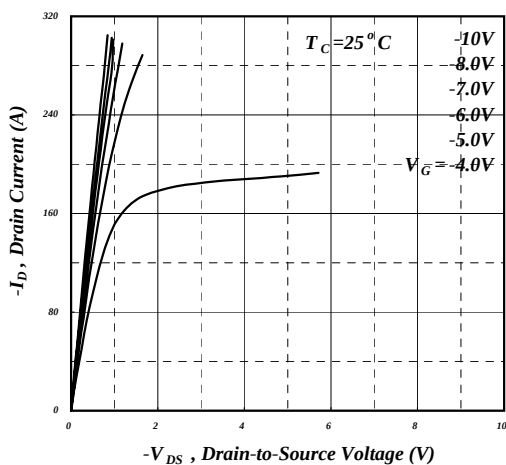
- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board, t ≤10sec
- 4.Package limitation current is 60A .
- 5.Starting T_j=25°C , V_{DD}=-30V , L=0.1mH , R_G=25Ω

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



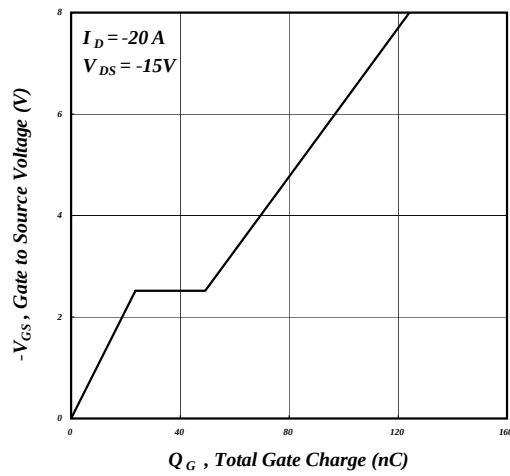


Fig 7. Gate Charge Characteristics

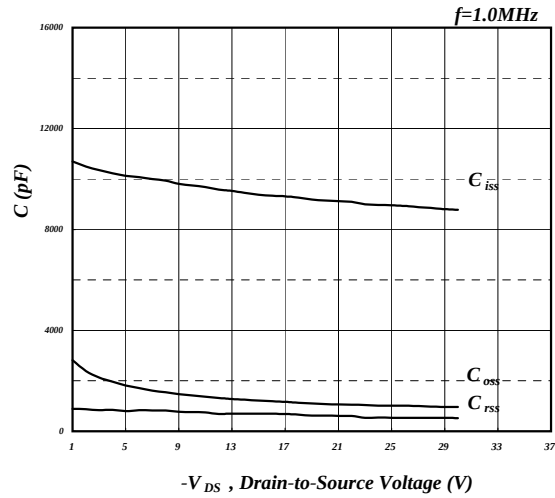


Fig 8. Typical Capacitance Characteristics

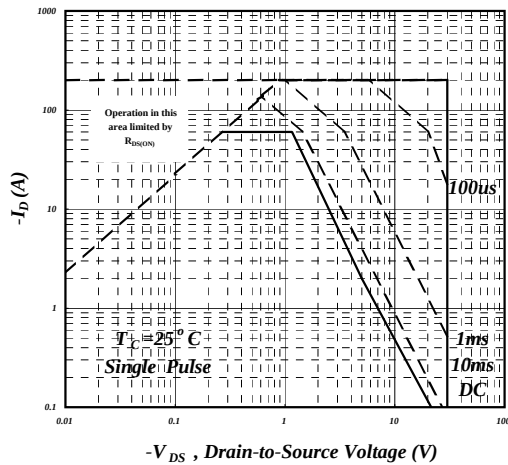


Fig 9. Maximum Safe Operating Area

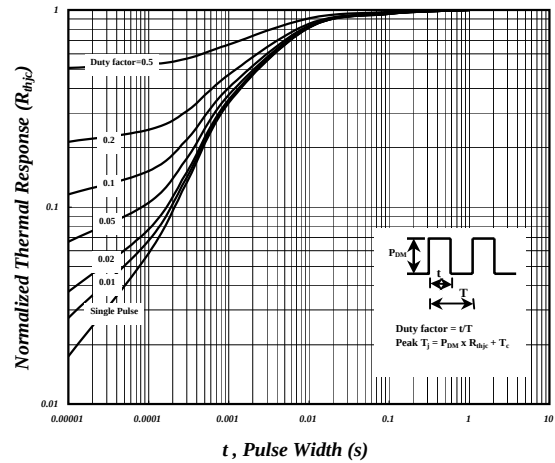


Fig 10. Effective Transient Thermal Impedance

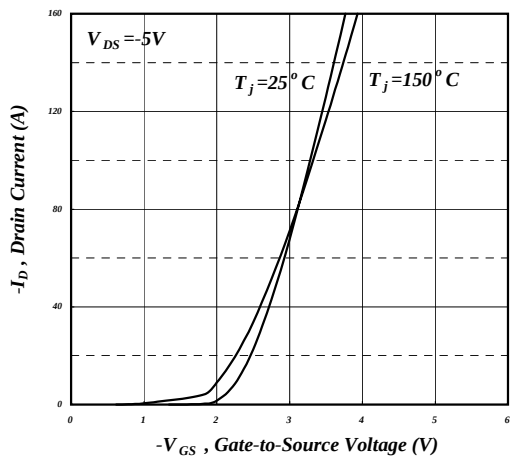


Fig 11. Transfer Characteristics

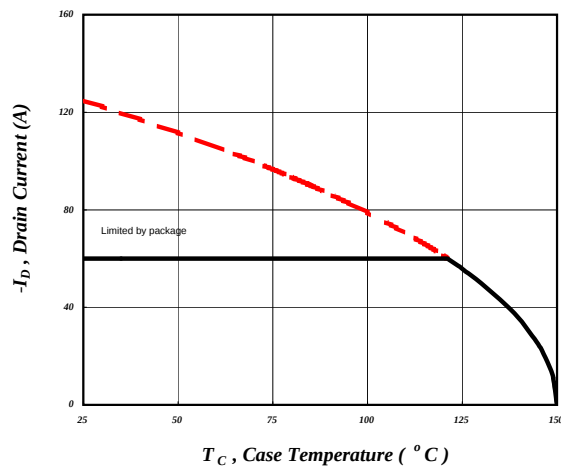


Fig 12. Drain Current v.s. Case Temperature

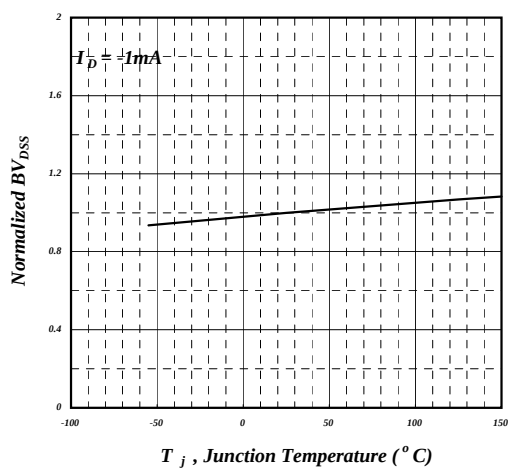


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

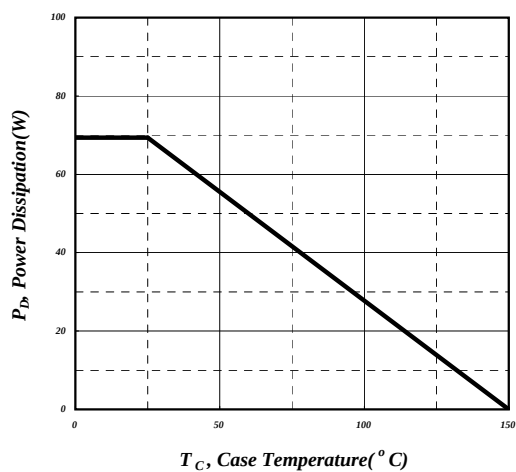


Fig 14. Total Power Dissipation

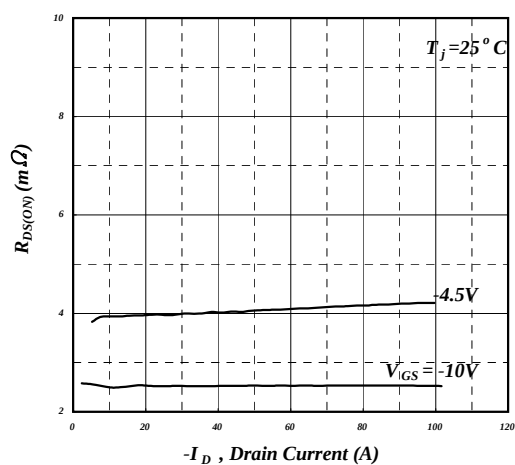


Fig 15. Typ. Drain-Source on State Resistance



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MARKING INFORMATION

