Intel® 500 Series Chipset Family Platform Controller Hub (PCH)

Specification Update

Revision 011

June 2023

Document Number: 635220-011

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Revision History

Document Number	Revision Number	Description	Revision Date
635220	011	• Added – Erratum 23 eSPI_CS1#, eSPI_CS2#, and eSPI_CS3# Floating Following Initial eSPI Reset Deassertion	June 2023
635220	010	• Updated – Erratum 13 - USB Audio Offload Traffic with Full-Speed Device Behind Hub • Added – Erratum 20 - USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst – Erratum 21 - G3 Current Specification on VCCRTC Rail – Erratum 22 - Timed GPIO Event May Have a Mismatched Time Stamp – Specification Clarification 4 - VCCRTC Voltage Requirement for G3 and Non-G3 State	July 2022
635220	009	• Updated – Stepping info in the Errata Summary table – Mobile Intel® IOTG Embedded Chipset HM570E, RM590E and QM580E identification; PCH stepping info in Identification Information chapter • Added – Specification Clarification 2 - SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled – Specification Clarification 3 - SATA Controller Support for Automatic Partial to Slumber Transition (APST) Feature	June 2022
635220	008	• Added – Erratum 17 - USB 2.0 Device Interrupt IN Endpoint Split Transaction Error – Erratum 18 - Processor C-States with USB Full-speed or Low-speed Device Hotplug – Erratum 19 - Leakage Current from VCCPRIM_1P8 Power Rail	February 2022
635220	007	• Updated – C0 stepping info in Identification Information chapter – C0 stepping info in Errata Summary table	December 2021
635220	006	• Added – Server Intel® Chipset C256 and C252 identification	November 2021

Document Number	Revision Number	Description	Revision Date
		– Erratum 14 - SLP_A# Minimum Assertion Width Timer During G3 Exit – Erratum 15 - xHCI Truncated Packet Detection with DPPABORT OS Framing – Erratum 16 - xHCI Force Header Command Incorrect Return Code • Updated – Erratum13 - USB Audio Offload Traffic with Full-Speed Device Behind Hub	
635220	005	• Added – Erratum12 - PCH and Processor Sync Error During C8 Entry – Erratum13 - USB Audio Offload Traffic with Full-Speed Device Behind Hub	September 2021
635220	004	• Updated – 1 Specification Clarification	July 2021
635220	003	• Added – Ring Oscillator Calibration – USB 3.2 Gen 1x2 Incorrect Retry Request – 1 Specification Clarification • Updated – PCIe* Clock and PCIe Reference Clock to Processor Maximum Rising/Falling Edge Rate and V_{CROSS} – xHCI Force Header Command	July 2021
635220	002	• Added Q570 and W580 in the Table 2-1.	May 2021
635220	001	• Initial Release	March 2021

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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents table. This document is a compilation of device and document errata and specification clarifications and changes. It is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into the specification update and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® 500 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 1 of 2	635218
Intel® 500 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 2 of 2	636174
Intel® 500 Series Chipset Family Platform Controller Hub (PCH) Electrical and Thermal Specifications	619122

1.2 Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

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2 Identification Information

2.1 Marking

Table 2-1. PCH Lines Component Identification

PCH Stepping	Top Marking (S-Spec)	Notes
B1	SRKM2	Desktop / Workstation Intel® Chipset H510
B1	SRKM5	Desktop / Workstation Intel® Chipset B560
B1	SRKM6	Desktop / Workstation Intel® Chipset H570
B1	SRKM3	Desktop / Workstation Intel® Chipset Z590
B1	SRKM4	Desktop / Workstation Intel® Chipset Q570
B1	SRKM7	Desktop / Workstation Intel® Chipset W580
B1	SRKM8	Server Intel® Chipset C256
B1	SRKM9	Server Intel® Chipset C252
B1	SRKMA	Mobile Intel® Chipset HM570
B1	SRKMB	Mobile Intel® Chipset WM590
B1	SRKMC	Mobile Intel® Chipset QM580
B1	SRKLS	Mobile Intel® IOTG Embedded Chipset HM570E
B1	SRKLR	Mobile Intel® IOTG Embedded Chipset RM590E
B1	SRKLT	Mobile Intel® IOTG Embedded Chipset QM580E

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3 Summary Tables of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

3.1 Codes Used in Summary Table

Stepping	Description
X	Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.
(No mark) or (Blank Box)	This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

3.2 Errata Summary Table

Erratum ID	PCH Stepping	Errata
	B1	
1	No Fix	Intel Trace Hub Pipe Line Empty
2	No Fix	SATA Enclosure Management LED Messaging
3	No Fix	eSPI SBLCL Register Bit Not Cleared by PLTRST#
4	No Fix	S0ix Entry When Connecting a USB-C* Power Adapter
5	No Fix	PCIe Clock and PCIe Reference Clock to Processor Maximum Rising/Falling Edge Rate and V_{CROSS}
6	No Fix	Integrated GbE Controller Reset on D3 Exit
7	No Fix	xHCI Link Protocol Field Value - USB 3.2 Gen 1x2 and 2x2
8	No Fix	USB VTIO Device Capabilities Field Length
9	No Fix	xHCI Force Header Command
10	Fixed	Ring Oscillator Calibration
11	No Fix	USB 3.2 Gen 1x2 Incorrect Retry Request
12	Fixed	PCH and Processor Sync Error During C8 Entry
13	No Fix	USB Audio Offload Traffic with Full-Speed Device Behind Hub
14	No Fix	SLP_A# Minimum Assertion Width Timer During G3 Exit
15	No Fix	xHCI Truncated Packet Detection with DPPABORT OS Framing
16	No Fix	xHCI Force Header Command Incorrect Return Code
17	Fixed	USB 2.0 Device Interrupt IN Endpoint Split Transaction Error

Erratum ID	PCH Stepping	Errata
	B1	
18	No Fix	Processor C-States with USB Full-speed or Low-speed Device Hotplug
19	No Fix	Leakage Current from VCCPRIM_1P8 Power Rail
20	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
21	No Fix	G3 Current Specification on VCCRTC Rail
22	No Fix	Timed GPIO Event May Have a Mismatched Time Stamp
23	No Fix	eSPI_CS1#, eSPI_CS2#, and eSPI_CS3# Floating Following Initial eSPI Reset Deassertion

3.3 Specification Changes

No.	Specification Changes
	No specification changes for this revision of the specification update.

3.4 Specification Clarifications

No.	Specification Clarifications
1	xHCI D3 Exit Timing
2	SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled
3	SATA Controller Support for Automatic Partial to Slumber Transition (APST) Feature
4	VCCRTC Voltage Requirement for G3 and Non-G3 State

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4 Errata Details

1	Intel Trace Hub Pipe Line Empty
Problem	The Intel Trace Hub Pipe Line Empty bit (CSR_MTB_BAR, Offset 0xD4) for a given output port may be set while the Input Buffer Empty for the associated output port is not set. This will only happen when the capture Done signal is de-asserted by clearing the ForceCaptureDone bit (CSR_MTB_BAR, Offset 0xD8) is cleared or the StoreQual[0] signal is de-asserted by the Trigger Unit before the pipe line is empty, and the destination is either system memory or USB (DCI).
Implication	There may be valid trace data in the trace source input buffer which did not get sent to the destination (output port).
Workaround	None identified. CaptureDone should be cleared or de-asserted after the pipe line is empty.
Status	For the steppings affected, refer to the Summary Table of Changes.

2	SATA Enclosure Management LED Messaging
Problem	When sending a SATA enclosure LED message and all SATA ports are either idle or disabled, the PCH may not transmit the LED message due to an internal clock gating issue.
Implication	The LED status for SATA enclosure may be incorrect.
Workaround	None identified. Enclosure Management SW can poll the Enclosure Management (EM_CTL) - Offset 20h bit 8 register for a 0 value immediately before writing LED messages.
Status	For the steppings affected, refer to the Summary Table of Changes.

3	eSPI SBLCL Register Bit Not Cleared by PLTRST#
Problem	The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.
Implication	If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.
Workaround	If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.
Status	For the steppings affected, refer to the Summary Table of Changes.

4	S0ix Entry When Connecting a USB-C* Power Adapter
Problem	Connecting a USB-C* power adapter to a PCH USB port may cause a race condition that can prevent the system from entering S0ix. This issue only occurs on designs where the USB-C Power Delivery (PD) implements Out Of Band (OOB) messaging to communicate with the PCH for port mapping.
Implication	The system may fail to enter S0ix.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

5	PCIe Clock and PCIe Reference Clock to Processor Maximum Rising/Falling Edge Rate and VCROSS
Problem	The PCIe Clock Output signals (CLKOUT_PCIE_P/N) and PCIe reference clock signals to processor (CLKOUT_CPUPCIBCLK_P/N) may not meet the maximum Rising/Falling Edge Rate and VCROSS specifications as defined in the PCI Express Card Electromechanical Specification Revision 3.0, section 2.1.3, REFCLK AC Specifications.
Implication	There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

6	Integrated GbE Controller Reset on D3 Exit
Problem	Upon GbE controller D3 exit, the GbE host driver performs a controller reset. During this reset, software accesses to the GbE MMIO registers may not complete.
Implication	The system may hang. *Note:* This erratum has only been observed in a synthetic environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

7	xHCI Link Protocol Field Value - USB 3.2 Gen 1x2 and 2x2
Problem	The xHCI Host Controller reports the value of 0h for the Link Protocol (LP) bits [15:14] in register XECP_SUPP_USB3_6 (MMIO offset 8038h) and XECP_SUPP_USB3_7 (MMIO offset 803Ch), which does not meet the xHCI specification revision 1.2.
Implication	There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

8	USB VTIO Device Capabilities Field Length
Problem	The xHCI spec version 1.2 defines the PCI Express Capability structure offset 04h Device Capabilities (DVSEC) field to be 8 bytes. The USB Virtualization Based Trusted IO (VTIO) Management controller implements the DVSEC field as 12 bytes.
Implication	A USB controller driver may not be able to enable the USB VTIO controller.
Workaround	None identified. To mitigate this erratum, an Independent Software Vendor could account for the field length in the USB controller driver.
Status	For the steppings affected, refer to the Summary Table of Changes.

9	xHCI Force Header Command
Problem	When USB 3.2 Gen 2x2 capability is enabled, the xHCI controller fails to execute the Force Header Command.
Implication	xHCI CV TD4.12 - Force Header Command Test may report an error. Intel has obtained a waiver for TD 4.12. *Note:* The Force Header Command is only used by the USB-IF Command Verifier (xHCI CV) tool for device testing. There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

10	Ring Oscillator Calibration
Problem	The PCH contains a ring oscillator calibration circuit to stabilize internal clocks across voltage and temperature changes. During operation, noise from the calibration circuit may cause the PCH internal clocks to deviate from expected frequency.
Implication	If the PCH internal clocks deviate from expected frequency, several unexpected behaviors may occur including system shutdown, system hang, or device detection issues.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

11	USB 3.2 Gen 1x2 Incorrect Retry Request
Problem	If a USB 3.2 Gen 2x2 device is operating at USB 3.2 Gen 1x2 speed and the device initiates a new data packet transfer within 6 idle symbols of a short packet completion, the xHCI controller may incorrectly send a retry request for the data packet with no host error bit set.
Implication	The data packet transfer from the device may stall and may require software to retry the data transfer request. *Note:* This issue has only been observed in a synthetic test environment. USB 3.2 Gen 2x2 devices will only operate at USB 3.2 Gen 1x2 speed due to signal degradation on the link.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

12	PCH and Processor Sync Error During C8 Entry
Problem	Due to an Internal PMC logic issue, the PCH and processor may become out of sync during C8 entry flow.
Implication	The system may hang.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

13	USB Audio Offload Traffic with Full-Speed Device Behind Hub
Problem	If USB audio offload is enabled for a USB Full-Speed Isochronous audio device connected behind a USB 2.0 or later hub and there is an active concurrent bulk transfer to another device on any port of the xHCI controller or behind the hub, the controller may stall the offloaded audio traffic and a split transaction error may occur.
Implication	The USB audio offload playback may stop. Audio may be recovered if the audio stream is paused and restarted, the audio device is removed and reconnected, or the audio application is restarted.
Workaround	None identified. A mitigation for this erratum is available with Intel® Smart Sound Technology version 10.29.00.5574 or later for systems with Microsoft Windows* 11 OS Release, or Intel Smart Sound Technology version 10.29.00.7767 or later for systems with Microsoft Windows 10 OS Release. This mitigation will disable audio offload functionality for USB audio devices connected behind a hub.
Status	For the steppings affected, refer to the Summary Table of Changes.

14	SLP_A# Minimum Assertion Width Timer During G3 Exit
Problem	Setting the Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP) bit (offset 1020h, bit 12 in PMC_MMIO space) to 1 does not disable the SLP_A# Minimum Assertion Width (SLP_A_MIN_ASST_WDTH) timer (offset 1020h, bit 17 and 16 in PMC_MMIO space).
Implication	G3 exit duration may be extended by the value programmed in the SLP_A_MIN_ASST_WDTH register.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

15	xHCI Truncated Packet Detection with DPPABORT OS Framing
Problem	The xHCI controller may not detect truncated packets from USB 3.2 Gen 1x1 hubs that send a truncated upstream packet with DPPABORT OS (Data Packet Payload Abort Order Set) framing.
Implication	A USB device connected behind a USB 3.2 Gen 1x1 Hub with this behavior may become unresponsive and require re-enumeration.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

16	xHCI Force Header Command Incorrect Return Code
Problem	The xHCI controller does not return the correct completion code for the Force Header Command as defined in the Section 4.6.16: Force Header of the eXtensible Host Controller Interface for Universal Serial Bus (xHCI) Requirements Specification, Revision 1.2.
Implication	xHCI CV TD4.12 - Force Header Command Test may report an error. Intel has obtained a waiver for TD 4.12. The Force Header Command is only used by the USB-IF Command Verifier (xHCI CV) tool for device testing. There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

17	USB 2.0 Device Interrupt IN Endpoint Split Transaction Error
Problem	When a USB Full-speed or Low-speed (with an Interrupt IN Endpoint) device is connected behind a USB hub, and a USB bulk device is also connected to any port on the xHCI controller, a split transaction error may occur on the USB Full-speed or Low-speed device.
Implication	The USB Controller driver may reset the USB Full-speed or Low-speed Interrupt IN Endpoint. The observed behavior is USB device specific. For example, a delay in response may be observed from a Low-speed USB mouse or keyboard device.
Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum. For a more power optimized solution, a xHCI controller driver may dynamically clear the xHCI MMIO offset 0x8144 bit 8 when a USB Full-speed or Low-speed device is not connected behind a USB Hub, and ensure the bit is set as configured by the BIOS.
Status	For the steppings affected, refer to the Summary Table of Changes.

18	Processor C-States with USB Full-speed or Low-speed Device Hotplug
Problem	When doing a hotplug on a USB hub with two or more USB Full-speed or Low-speed devices each with a 1 ms service interval interrupt endpoint, a race condition may occur between the PMC and the xHCI controller.
Implication	The processor may fail to enter C3 or deeper package C-States. *Note:* This erratum has only been observed in a synthetic environment.
Workaround	None identified. This condition is recovered after the xHCI controller has successfully entered D3.
Status	For the steppings affected, refer to the Summary Table of Changes.

19	Leakage Current from VCCPRIM_1P8 Power Rail
Problem	When the VCCPRIM_1P8 is off and the VCCPRIM_3P3 is powered on during G3 to S5, there may be a leakage current from the VCCPRIM_3P3 power rail to VCCPRIM_1P8 power rail.
Implication	The leakage voltage may be observed on VCCPRIM_1P8 power rail. There is no known functional or reliability impact.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

20	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect two LFPS signals. This issue may impact the SuperSpeed compliance test case, which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.

Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

21	**G3 Current Specification on VCCRTC Rail**
Problem	The PCH VCCRTC current draw during the G3 state may exceed the maximum current specification of 6 µA, as documented in the *Intel® 500 Series Chipset Family Platform Controller Hub Datasheet – Volume 1 of 2* (Document number: 635218).
Implication	PCH units may experience VCCRTC rail current draw during the G3 state up to 8 uA. Platform implications are platform design specific.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

22	**Timed GPIO Event May Have a Mismatched Time Stamp**
Problem	When a Timed GPIO event is counted in the Event Counter Capture (TGPIOECCV) register (offset 1238h, bits 31 to 0 in PWRMBASE space), the Time Capture (TGPIOTCV) register (offset 1230h, bits 31 to 0 in PWRMBASE space) value is not immediately updated after that event is counted.
Implication	A Timed GPIO event may have a mismatched time stamp.
Workaround	None identified. A Timed GPIO driver can partially mitigate for this erratum by detecting that a TGPIOECCV register change has occurred without a TGPIOTCV register change, and then repeatedly re-read the TGPIOTCV register until a change occurs.
Status	For the steppings affected, refer to the Summary Table of Changes.

23	**eSPI_CS1#, eSPI_CS2#, and eSPI_CS3# Floating Following Initial eSPI Reset Deassertion**
Problem	During Deep Sx exit or booting from G3 state, eSPI_CS1#, eSPI_CS2#, and eSPI_CS3# are momentarily high impedance and may float low following the initial eSPI_RESET# deassertion.
Implication	Due to this erratum, unexpected system behavior may occur on systems with more than one eSPI device.
Workaround	Implement 10 kΩ external pull-Up resistors to the VCCPRIM_1P8 voltage rail on eSPI_CS1#, eSPI_CS2#, and eSPI_CS3#.
Status	For the steppings affected, refer to the Summary Table of Changes.

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5 Specification Changes

There are no specification changes in this revision of the Specification Update.

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6 Specification Clarification

1	**xHCI D3 Exit Timing**
	Add the following text to the *Intel® 500 Series Chipset Family Platform Controller Hub (PCH) Datasheet Volume 2 of 2* (Document Number: 636174) in the Power Management Control/Status (PM_CS) register summary, bits 1:0, 'PowerState (POWERSTATE)' field description section: "**Software should wait for 100 ms before requesting the xHCI controller to re-enter D3 after a D3 exit.**"
2	**SX_EXIT_HOLDOFF# Not Functional with eSPI Enabled**
	Add the following note to the *Intel® 500 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 1 of 2* (Document Number: 635218) in the SX_EXIT_HOLDOFF# Signal Description in the Power Management chapter Signal Description section: **"When eSPI is enabled, the flash sharing functionality using SX_EXIT_HOLDOFF# is not supported, but the pin still functions to hold off Sx exit after SLP_A# de-assertion."**
3	**SATA Controller Support for Automatic Partial to Slumber Transition (APST) Feature**
	Add the following note to the *Intel® 500 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 2 of 2* (Document Number: 636174) in the HBA Capabilities Extended (GHC_CAP2) register summary, bit 2, 'Automatic Partial to Slumber Transitions (APST)' field description section: **"BIOS should set this bit to 0 as APST is not supported."**
4	**VCCRTC Voltage Requirement for G3 and Non-G3 State**
	Update the following table row to the *Intel® 500 Series Chipset Family Platform Controller Hub (PCH) Electrical and Thermal Specifications* (Document number: 619122) in the VCCRTC section of Power Rails Spec sheet:

Symbol	Parameter	Minimum	Nominal	Maximum	Unit
VCCRTC	RTC Well Supply (non-G3)	3.135	3.3	3.465	V
VCCRTC	RTC Well Supply (G3)	2.0	3.0	3.465	V

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