4/3/2/1+2/1/0-Phase PWM Controller with SMBus Digital Interface for FM2+ CPU Core Power

General Description

The uP9505 is an AMD SVI2 compliant desktop CPU voltage regulator controller that integrates a 4-phase PWM controller for VDD and a 2-phase controller for VDDA. The VDD controller can be configured as 4/3/2/1-phase, and the VDDA controller can be configured as 2/1/0-phase (0 denotes VDDA controller is disabled) for platform power design flexibility. For the typical 4+2-phase application, the 4-phase VDD controller has 4 PWM outputs. The 2-phase VDDA controller has 2 PWM outputs. The controller provides further flexible operating phase configurations to support 6+0 or 5+1 phase application (0 denotes VDDA controller is disabled). The integrated SMBus interface programmability makes this part with high performance and easy design. Designer can define different power scenario for different current states to optimize the performance and efficiency.

The uP9505 combines true differential output voltage sense, differential inductor DCR current sense, input voltage feed-forward sense and adaptive voltage positioning to provide accurately regulated power for desktop CPU. It adopts uPI proprietary RCOT+™ (Robust Constant On-Time) topology to have fast transient response and smooth mode transition. Similar to digital based PWM controller, the loop gain is also programmable by SMBus interface to achieve design flexibility.

The uP9505 has built-in serial interface to communicate with AMD SVI2 compliant CPU. It supports mode transition function with various operating states. This part provides two different VID on-the-fly slew rates, which can be programmed by the SMBus register.

The uP9505 provides power good indicator and selectable VR parameters, such as SMBus device address and Vboot voltage. It also provides complete fault protection functions, including over voltage, under voltage, over current, over temperature and under voltage lockout. The uP9505 is available in VQFN6x6-52L package.

Ordering Information

Order Number	Package	Remark
uP9505PQGW	VQFN6x6-52L	

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) p lating that are suitable for use in SnPb or Pb-free soldering processes.

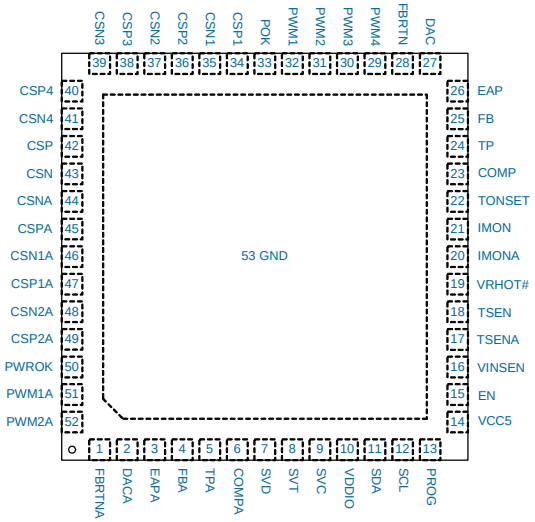
Features

- AMD SVI2 CPU Compliant
- RCOT+™ Control Topology
  - Easy Setting
  - Smooth Mode Transition
  - Fast Transition Response
- Flexible Operation Phase Configuration
  - 4/3/2/1-Phase PWM Controller for VDD
  - 2/1/0-Phase PWM Controller for VDDA
  - Support Operation Phase Disable Function
  - Support 6+0 or 5+1 Phase Application
- SMBus Interface for Performance and Efficiency Optimization
  - Dynamic Programmable VR Parameters
  - Programmable Protection Thresholds
  - VR Output Reporting
  - Programmable Loop Gain
- Programmable Operation Frequency
- Inductor DCR Current Sensing for Droop/ Channel OCP/ Total OCP
- Differential Current Sense Amplifier for Current Balance
- Differential Remote Output Voltage Sense
- Transient Boost for Fast Transient Response
- High Accuracy DAC
- OCP/UVP/OVP/Thermal Shutdown
- RoHS Compliant and Halogen Free

Applications

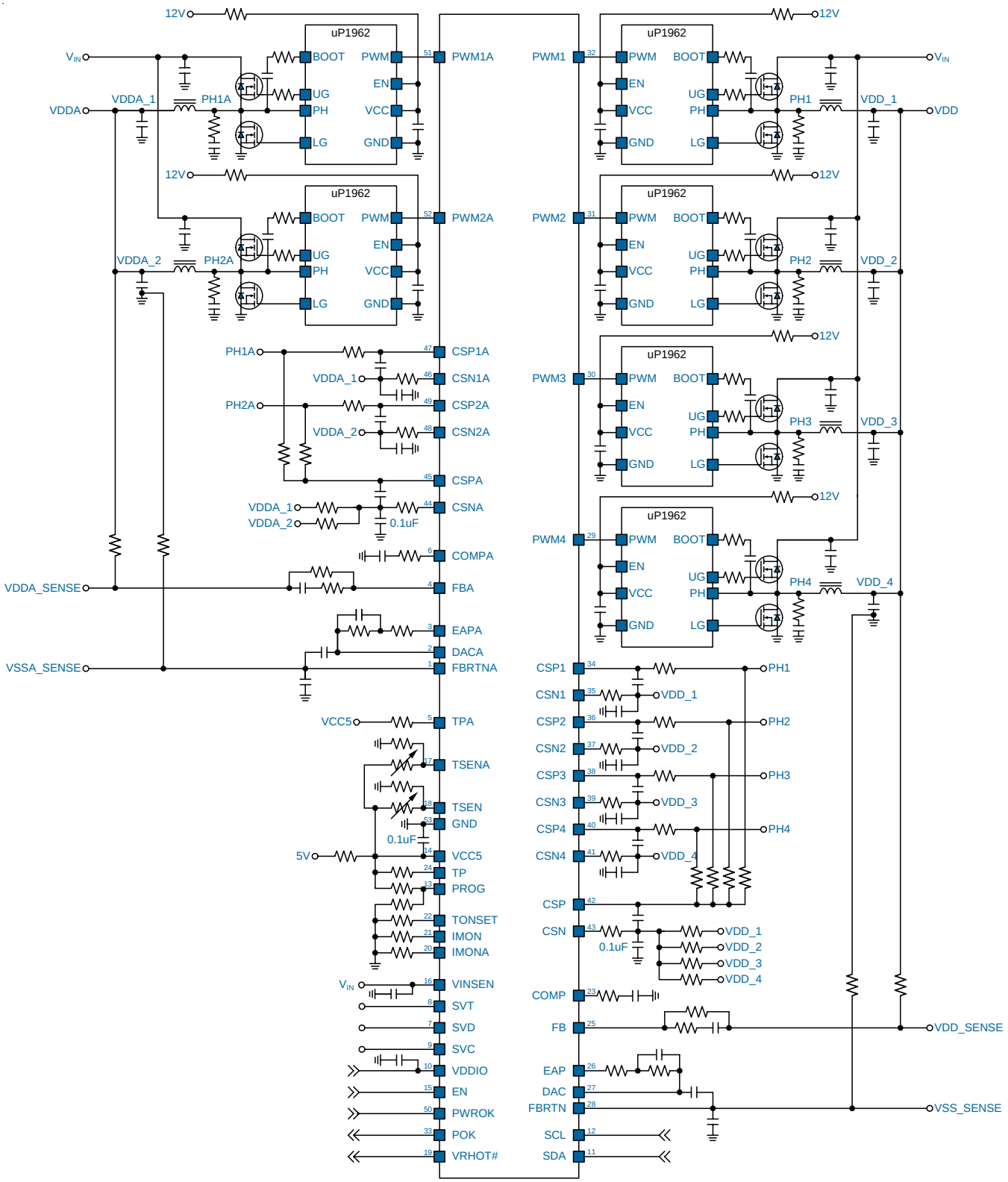
- AMD FM2+ Desktop CPU Power Supplies
- AMD VGA Card GPU Power Supplies

Pin Configuration



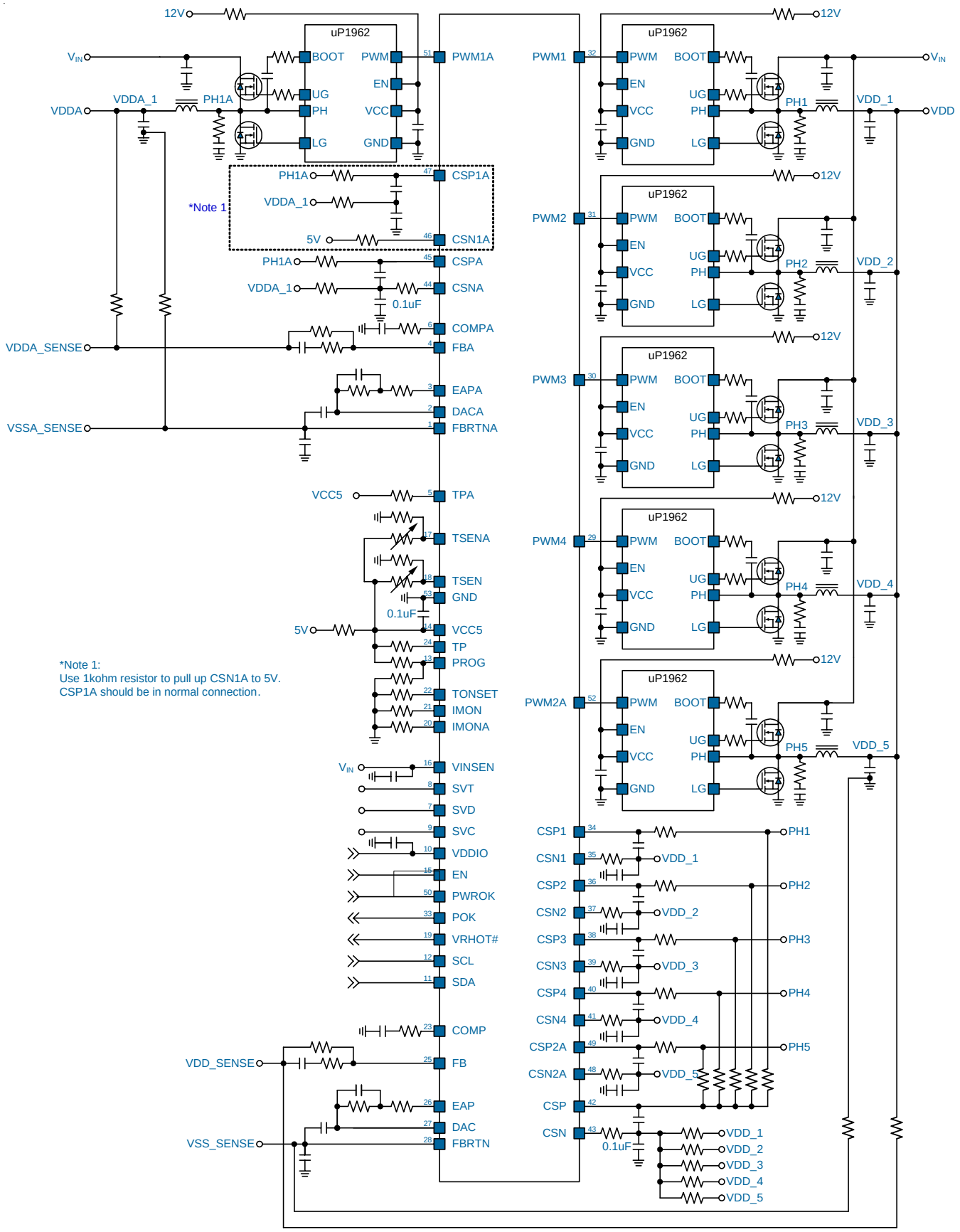
Typical Application Circuit

4+2 Phase Application



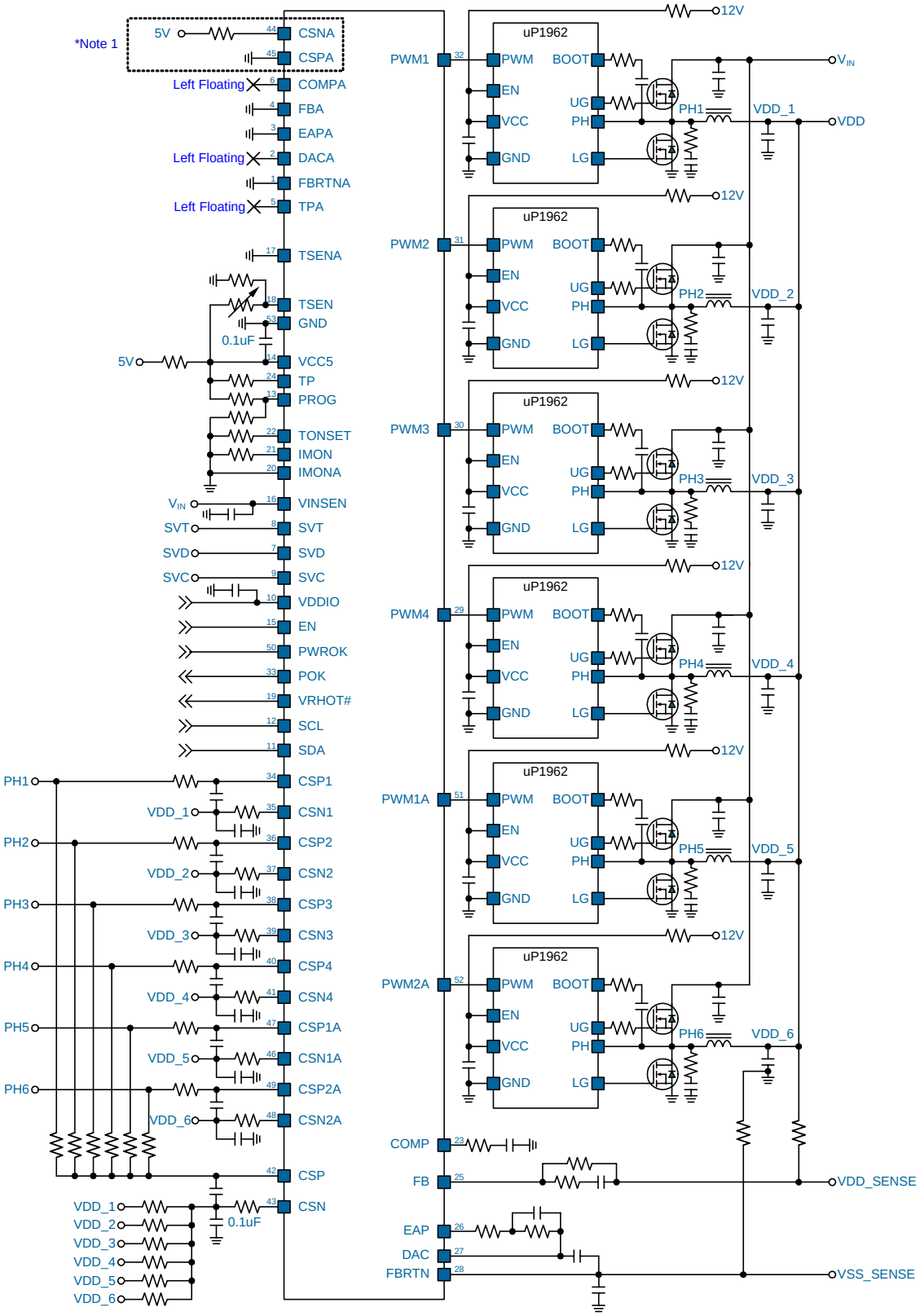
Typical Application Circuit

5+1 Phase Application



Typical Application Circuit

6+0 Phase Application



*Note 1:
Use 1kΩ resistor to pull up CSNA to 5V.
Connect CSPA to ground.

Functional Pin Description

No.	Name	Pin Function
1	FBRTNA	**Output Voltage Feedback Return for VDDA.** Inverting input to the differential voltage sense amplifier. FBRTNA is the reference point in DACA output voltage measurement. Connect this pin directly to the processor output voltage feedback return sense point, namely VSSA_SENSE.
2	DACA	**DAC Output for VDDA.** The output voltage of this pin is the reference voltage for the VDDA rail. DACA voltage is measured with respect to FBRTNA. Connect a capacitor from this pin to FBRTNA.
3	EAPA	**Non-Inverting Input of the Error Amplifier for VDDA.** Connect a resistor between this pin and DACA to set the droop (load line) function.
4	FBA	**Inverting Input of the Error Amplifier for VDDA.**
5	TPA	**Test Pin for VDDA.** Reserved for VDDA internal testing purpose.
6	COMPA	**Output of Control Loop Error Amplifier for VDDA**. Connect a resistor in series with a capacitor from this pin to GND for voltage control loop compensation.
7	SVD	**Serial VID Data.** SVD is a push-pull with high-Z output of the processor. SVD can be driven by the VR during the Acknowledgement phase.
8	SVT	**Serial VID Telemetry.** SVT is a push-pull output of the processor.
9	SVC	**Serial VID Clock.** SVC is a push-pull output of the processor.
10	VDDIO	**The reference for the processor for the memory interface.** Connect a capacitor between VDDIO and GND to power and reference the SVC, SVD, SVT pins.
11	SDA	**SMBus Data Input.** This pin is input or output of serial bus data signal.
12	SCL	**SMBus Clock Input.** This pin receives serial bus clock signal input**.**
13	PROG	**Function Setting Pin**. Connect a resistor voltage divider from VCC5 to GND to set the initial start up voltage (Vboot) for VDDA and SMBus device address.
14	VCC5	**Supply Input for Logic Control Circui**t. Connect this pin to a 5V voltage source via an RC filter. VCC5 is the supply input for the logic control circuit.
15	EN	**Chip Enable Control Input**. Pull this pin above 2V enables the chip. Pull this pin below 0.8V to disable the chip.
16	VINSEN	**Power Stage Input Voltage Sense.** Directly connect this pin to the power stage input V_{IN}. The controller senses the voltage on this pin for power stage input voltage V_{IN} detection. The VINSEN voltage is also used for PWM on-time calculation.
17	TSENA	**Thermal Sensing for VDDA.** Connect NTC network to this pin for thermal sensing. The controller uses specific nonlinear A/D converter in thermal reporting. The recommended NTC thermistor is 10kΩ/β= 3380 by Murata (NCP18XH103F03RB), and the recommended lower dividing resistor is 6kΩ.
18	TSEN	**Thermal Sensing for VDD.** Connect NTC network to this pin for thermal sensing. The controller uses specific nonlinear A/D converter in thermal reporting. The recommended NTC thermistor is 10kΩ/β= 3380 by Murata (NCP18XH103F03RB), and the recommended lower dividing resistor is 6kΩ.
19	VRHOT#	**VRHOT# Output.** This pin is an open-drain output. The controller asserts VRHOT# when the sensed temperature is higher than the value of SMBus register 0x29h (TEMP_VRHOT), in which the default value is 05h (106°C)

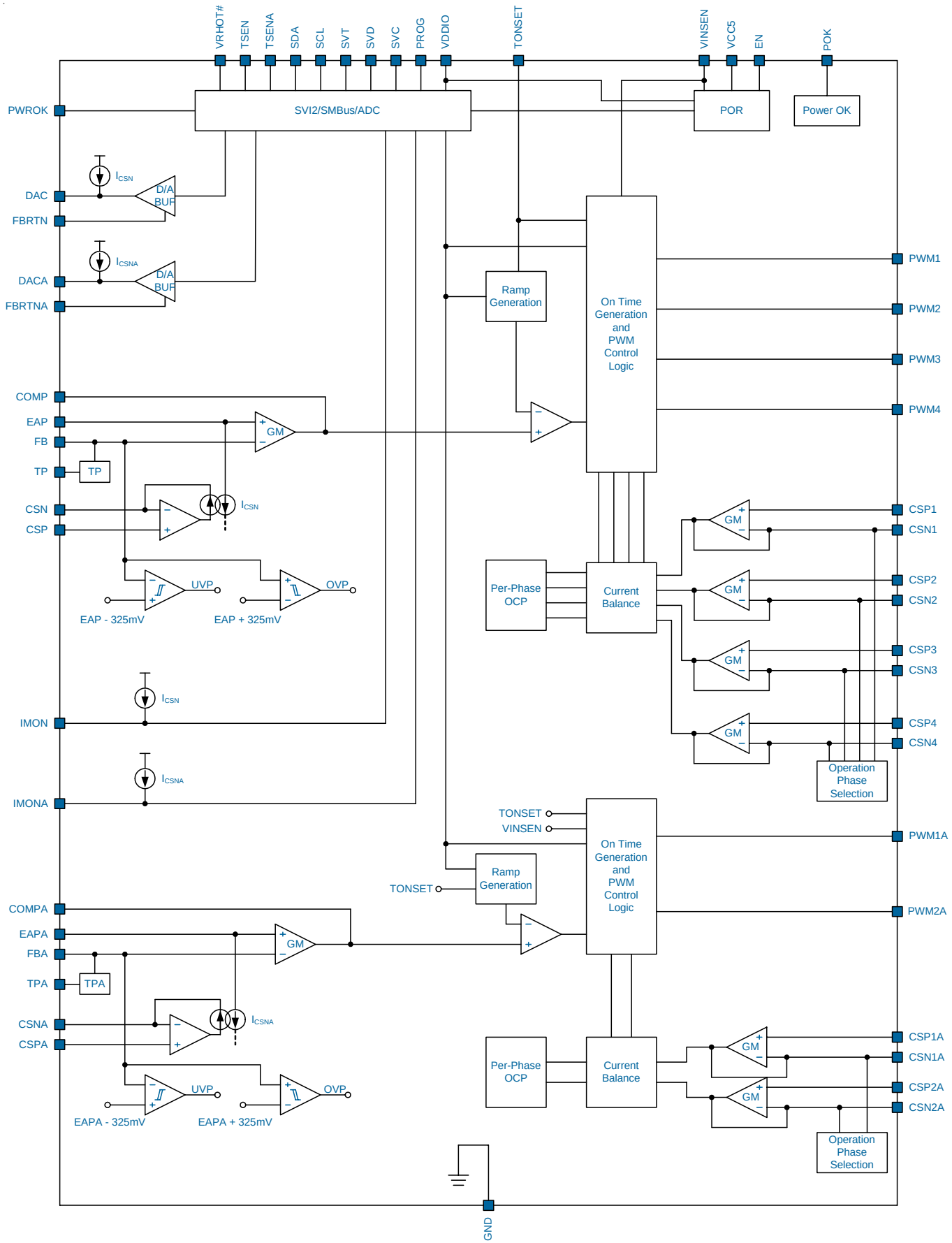
Functional Pin Description

No.	Name	Pin Function
20	IMONA	**Over Current Protection Threshold Setting and Sensing for VDDA**. Connect a resistor from this pin to GND to set the over current protection threshold. Do not connect any capacitor to this pin. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the IMONA voltage proportional to the total output current. When the voltage on IMONA pin exceeds 2.56V, the over current protection will be tripped to shutdown the controller.
21	IMON	**Over Current Protection Threshold Setting and Sensing for VDD.** Connect a resistor from this pin to GND to set the over current protection threshold. Do not connect any capacitor to this pin. The output current of this pin is proportional to the total load current. The total load current is sensed and flows out of this pin, and a resistor from this pin to GND makes the IMON voltage proportional to the total output current. When the voltage on IMON pin exceeds 2.56V, the over current protection will be tripped to shutdown the controller.
22	TONSET	**PWM On-Time Setting.** Connect a resistor from this pin to GND to set the PWM on-time. The VDD VR and VDDA VR share the same PWM on-time setting.
23	COMP	**Output of Control Loop Error Amplifier for VDD**. Connect a resistor in series with a capacitor from this pin to GND for voltage control loop compensation.
24	TP	**Test Pin for VDD.** Reserved for VDD internal testing purpose.
25	FB	**Inverting Input of the Error Amplifier for VDD.**
26	EAP	**Non-Inverting Input of the Error Amplifier for VDD**. Connect a resistor between this pin and DAC to set the droop (load line) function**.**
27	DAC	**DAC Output for VDD.** The output voltage of this pin is the reference voltage for the VDD rail. DAC voltage is measured with respect to FBRTN. Connect a capacitor from this pin to FBRTN.
28	FBRTN	**Output Voltage Feedback Return for VDD.** Inverting input to the differential voltage sense amplifier. FBRTN is the reference point in DAC output voltage measurement. Connect this pin directly to the processor output voltage feedback return sense point, namely VSS_SENSE.
29	PWM4	**VDD Phase 4 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. This pin outputs a PWM logic signal for external discrete MOSFET driver for VDD rail
30	PWM3	**VDD Phase 3 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. This pin outputs a PWM logic signal for external discrete MOSFET driver for VDD rail.
31	PWM2	**VDD Phase 2 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. This pin outputs a PWM logic signal for external discrete MOSFET driver for VDD rail
32	PWM1	**VDD Phase 1 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. This pin outputs a PWM logic signal for external discrete MOSFET driver for VDD rail.
33	POK	**Power OK Indication.** This pin is an open-drain output that indicates the VDD/VDDA start up to output voltage Vboot and no fault happens**.**
34	CSP1	**Positive Differential Current Sense Input for VDD Phase 1.**
35	CSN1	**Negative Differential Current Sense Input for VDD Phase 1.**
36	CSP2	**Positive Differential Current Sense Input for VDD Phase 2.** When VDD phase 2 is not used, short this pin to GND when VDD VR is configured in single-phase configuration.
37	CSN2	**Negative Differential Current Sense Input for VDD Phase 2.** When VDD phase 2 is not used, pull high this pin to VCC5 through a 1kΩ resistor to disable PWM2 to let VDD VR operate in single-phase configuration.

Functional Pin Description

No.	Name	Pin Function
38	CSP3	**Positive Differential Current Sense Input for VDD Phase 3.** When VDD phase 3 is not used, short this pin to GND when VDD VR is configured in 2-phase configuration.
39	CSN3	**Negative Differential Current Sense Input for VDD Phase 3.** When VDD phase 3 is not used, pull high this pin to VCC5 tthrough a 1kΩ resistor to disable PWM3 to let VDD VR operate in 2-phase configuration.
40	CSP4	**Positive Differential Current Sense Input for VDD Phase 4.** When VDD phase 4 is not used, short this pin to GND when VDD VR is configured in 3-phase configuration.
41	CSN4	**Negative Differential Current Sense Input for VDD Phase 4.** When VDD phase 4 is not used, pull high this pin to VCC5 through a 1kΩ resistor to disable PWM4 to let VDD VR operate in 3-phase configuration.
42	CSP	**Non-Inverting Input of Total Current Sense Amplifier for VDD.**
43	CSN	**Inverting Input of Total Current Sense Amplifier for VDD.**
44	CSNA	**Inverting Input of Total Current Sense Amplifier for VDDA.**
45	CSPA	**Non-Inverting Input of Total Current Sense Amplifier for VDDA.**
46	CSN1A	**Negative Differential Current Sense Input for VDDA Phase 1.** When VDDA phase 1 is not used, pull high this pin to VCC5 through a 1kΩ resistor to disable PWM1A to let VDDA VR operate in zero-phase configuration.
47	CSP1A	**Positive Differential Current Sense Input for VDDA Phase 1.** When VDDA phase 1 is not used, short this pin to GND when VDDA VR is configured in zero-phase configuration.
48	CSN2A	**Negative Differential Current Sense Input for VDDA Phase 2.** When VDDA phase 2 is not used, pull high this pin to VCC5 through a 1kΩ resistor to disable PWM2A to let VDDA VR operate in single-phase configuration.
49	CSP2A	**Positive Differential Current Sense Input for VDDA Phase 2.** When VDDA phase 2 is not used, short this pin to GND when VDDA VR is configured in single-phase configuration.
50	PWROK	**System Power OK Indication.** This pin is the active high that indicates the system power is ok. When PWROK is asserted, it indicates that all voltage planes and free-running clocks are within specification.
51	PWM1A	**VDDA Phase 1 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. This pin outputs a PWM logic signal for external discrete MOSFET driver for VDDA rail.
52	PWM2A	**VDDA Phase 2 PWM Output.** Connect this pin to the PWM input of external MOSFET driver. This pin outputs a PWM logic signal for external discrete MOSFET driver for VDDA rail.
Exposed Pad		**Ground.** The exposed pad is the ground of all logic control circuits, and it must be soldered to a large PCB and connected to GND.

Functional Block Diagram



Power Input and Power On Reset

The uP9505 has a single power input VCC5. VCC5 is the 5V supply input for control logic circuit of the controller. RC filter to VCC5 is required for locally bypassing this supply input. The controller monitors the VINSEN voltage for PWM on-time calculation. EN is the chip enable input pin. Logic high to this pin enables the controller, and logic low to this pin disables the controller. The above three inputs (VCC5, VINSEN and EN) are monitored to determine whether the controller is ready for operation.

Figure 1 shows the power ready detection circuit. The VCC5 voltage is monitored for power on reset with typically 4.3V threshold at its rising edge.The VINSEN voltage is monitored for power on reset with typically 6V threshold at its rising edge. The VDDIO voltage is monitored for power on reset with typically 0.8V threshold at its rising edge. When VCC5, VDDIO and VINSEN are all ready, the controller waits for EN to start up. When EN pin is driven above 2V, the controller begins its start up sequence. When EN pin is driven below 0.8V, the controller will be turned off, and it will clear all fault states to prepare to next start up once the controller is re-enabled. Note that only VCC5 or EN toggle will clear all fault state, VDDIO or VINSEN toggle is not used for clearing fault state. Anytime any one of the four inputs falls below their power on reset level will shutdown the controller.

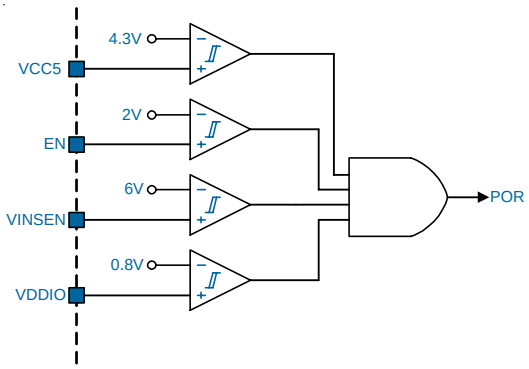


Figure 1. Circuit for Power Ready Detection

Power-up Sequence

Figure 2 shows a typical power-up sequence of uP9505. When VCC5, VDDIO and VINSEN inputs are all ready, the controller waits for the EN signal to initiate the power on sequence. After EN goes high, the controller waits for a delay time T_A (<1ms) then the output voltage starts to ramp up to Vboot. The time interval T_B is determined by the VID upward slew rate. The uP9505 asserts POK when VDD/ VDDA rails are in regulation of the voltage (Vboot).

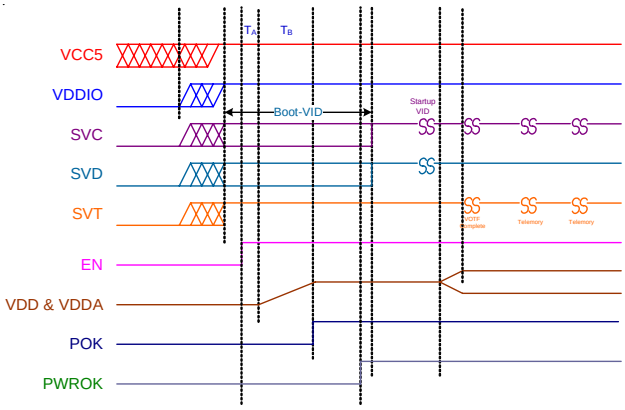


Figure 2. Power Up Sequence Timing

Initial Start Up Voltage (Vboot) and SMBus Device Address (PROG)

Refer to the Table 1. The uP9505 determines the Vboot voltage upon the SVC and SVD status during POR.

Table 1. Vboot Voltage for both VDD and VDDA

SVC	SVD	Vboot
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

The uP9505 features selectable initial start up voltage (Vboot) and SMBus device address for design flexibility. PROG is a function setting pin, which is used to set the two essential parameters. Refer to Figure 3, connect a resistor voltage divider to the PROG pin to set the initial start up voltage (Vboot) for VDDA and SMBus device address. The VDDA Vboot can be set to 1.55V, 1.5V, 1.35V, and follow SVI2 connections. The SMBus device address can be set to 0x88h, or 0x8Ah. Table 2 shows the recommended resistance value for PROG function setting.

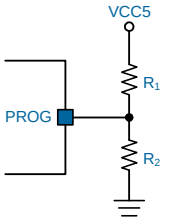


Figure 3 Initial Parameter Setting

Table 2.PROG Resistor Setting

VDDA Vboot (V)	SMBus Address	R1/R2 Resistor Value (kΩ)					
		4+2 Phase		5+1 Phase		6+0 Phase	
		R1	R2	R1	R2	R1	R2
1.55	88	4.92	3.37	24.61	16.84	NA	NA
1.5	88	4.27	3.77	21.33	18.83	NA	NA
1.35	88	3.76	4.27	18.82	21.34	NA	NA
Follow SVI2 Connections (Table 1)	88	3.37	4.92	16.84	24.62	30.31	44.31
1.55	8A	3.05	5.82	15.24	29.1	NA	NA
1.5	8A	2.78	7.11	13.91	35.56	NA	NA
1.35	8A	2.56	9.14	12.8	45.72	NA	NA
Follow SVI2 Connections (Table 1)	8A	2.37	12.8	11.85	64.02	21.33	115.24

Operation Phase Disable Function

The uP9505 supports operation phase disable function to further increase the design flexibility. Platform designer can choose to disable some phases to meet their design requirement. Both VDD and VDDA rail support operation phase disable function. The minimum operation phase number is 1+0-phase. In general, to disable a specific phase, pull up CSNx to VCC5 through 1kΩ resistor and tie CSPx to ground for that phase. The controller detects all the CSNx voltage at VCC5 power on reset to determine operation phase number.

Note that there is an exception for VDDA rail phase disable function. To let VDDA rail in zero-phase operation, pull up CSNA to VCC5 through 1kΩ resistor and tied CSPA to ground. Table 4 shows the operation phase number setting.

In addition, the operating phase number is governed by the SVI2 command. The SVI2 command and operating phase number are shown as Table 3.

Table 3. SVI2 Command and VDD & VDDA Operating Phase Number

PSI0_L	PSI1_L	Set VDD Phase Number	Set VDDA Phase Number
1	1	Full Phase CCM	Full Phase CCM
1	0	Full Phase CCM	Full Phase CCM
0	1	1 Phase CCM	1 Phase CCM
0	0	1 Phase PSM	1 Phase PSM

Table 4. Operation Phase Number Setting

Configuration	Supported Operation Phase Number	Pin connection, Pull High/ Pull Low to Target											
		CSPA	CSNA	CSP4	CSN4	CSP3	CSN3	CSP2	CSN2	CSP2A	CSN2A	CSP1A	CSN1A
4+2-Phase	4+2	--	--	--	--	--	--	--	--	--	--	--	--
	5+1	--	--	--	--	--	--	--	--	--	--	(Note 5)	VCC5
	6+0	GND	VCC5	--	--	--	--	--	--	--	--	--	--
	3+2			GND	VCC5	--	--	--	--	--	--	--	--
	5+0	GND	VCC5	--	--	--	--	--	--	--	--	GND	VCC5
	4+1	--	--	--	--	--	--	--	--	GND	VCC5	--	--
	4+0	GND	VCC5	--	--	--	--	--	--	GND	VCC5	GND	VCC5
	3+1	--	--	GND	VCC5	--	--	--	--	GND	VCC5	--	--
	2+2	--	--	GND	VCC5	GND	VCC5	--	--	--	--	--	--
	3+0	GND	VCC5	GND	VCC5	--	--	--	--	GND	VCC5	GND	VCC5
	2+1	--	--	GND	VCC5	GND	VCC5	--	--	GND	VCC5	--	--
	2+0	GND	VCC5	GND	VCC5	GND	VCC5	--	--	GND	VCC5	GND	VCC5
	1+1	--	--	GND	VCC5	GND	VCC5	GND	VCC5	GND	VCC5	--	--
	1+0	GND	VCC5	GND	VCC5	GND	VCC5	GND	VCC5	GND	VCC5	GND	VCC5

Note 1. "--" denotes normal connection.
Note 2. Use 1kΩ pull up resistor when pull-up to VCC5
Note 3. Pay attention to the CSNA connection when using phase disable function of VDDA rail in zero phase configuration.
Note 4. Strictly follow the table for phase disable. Incorrect PROG setting and incorrect pin pull up/down connection will cause catastrophic fault during start-up.
Note 5. For 5+1 phase operation. CSP1A should be in normal connection.

PWM On-Time Setting

The PWM on-time is set by an external resistor R_{TON} connected between TONSET pin and GND. The controller senses VINSEN voltage to obtain input voltage information for PWM on-time calculation. Both the VDD rail and VDDA rail share the same PWM on-time setting. The PWM on time can be calculated as below equation.

$$T_{ON} = \left(\frac{V_{OUT}}{V_{IN}} \right) \times R_{TON} \times 100$$

where T_{ON} is in ns, R_{TON} is in kΩ.
Table 5 lists the switching frequency and the recommended resistor R_{TON} value (with condition: V_{IN} = 12V, V_{OUT} = 1.2V). For example, given V_{IN} = 12V, V_{OUT} = 1.2V, R_{TON} = 49.9kΩ, T_{ON} is about 500ns by above equation. The PWM frequency is about 200kHz. Note that the resistance value of R_{TON} value must be greater than 10kΩ to ensure the PWM on time calculation circuit in normal operation.

Table 5. Switching Frequency and Resistor R_{TON}

Switching Frequency (kHz)	Recommended Resistor R_{TON} (kΩ)
200	49.9
300	33
400	24.9
500	20
600	16
Note: The minimum of resistor R_{TON} value is 10kΩ.	

DAC Reference Voltage

The uP9505 embeds separate precise bandgap reference voltage generation circuits for VDD and VDDA controllers. Figure 4 shows the reference voltage generation circuit. The output voltage of bandgap reference circuit is 1.55V with respect to FBRTN (FBRTNA for VDDA).

The uP9505 utilizes plural resistors to generate precise reference voltages ranging from 6.25mV to 1.55V, with 6.25mV step. All the voltages connect to a multiplexer (MUX). According to SVI2 command, the MUX outputs the selected VID (VDAC) to the current limit buffer input. The DAC voltage is generated as the reference voltage to the DAC pin (DACA pin for VDDA). The DAC voltage for VDDA is generated by the same method except that it is referred to FBRTNA pin. Table 6 shows the VID voltage and the SVI2 code.

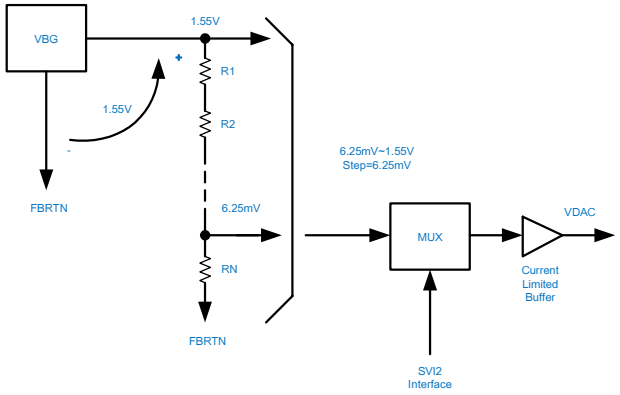


Figure 4. Reference Voltage Generation Circuit

Dynamic VID Change and Slew Rate

The controller accepts SetVID command via SVI2 bus for output voltage change during normal operation. This allows the output voltage to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (VID OTF). A VID OTF event may occur under either light or heavy load condition. This voltage change direction can be upward or downward. The default value of VID upward slew rate is 12mV/us. The value of VID downward slew rate is 1/3 of VID upward slew rate. The upward slew rate of VDD and VDDA can be separately further programmed by the controllers SMBus register 0x26h. The upward slew rate can be set from 8mV/us to 22mV/us with a total of 7 steps and 2mV/LSB resolution. The default value of upward slew rate is 12mV/us.

Output Voltage Differential Sense

The uP9505 uses differential sense by a high-gain low offset error amplifier for output voltage differential sense as shown in Figure 5. The CPU voltage is sensed by the FB and FBRTN pins (FBA and FBRTNA for VDDA). FB pin is connected to the positive remote sense pin VDD_SENSE of the CPU via the resistor R_{FB}. FBRTN pin is connected to the negative remote sense pin VSS_SENSE of CPU directly. (VDDA_SENSE and VSSA_SENSE for VDDA).

The error amplifier compares the V_{FB} with V_{EAP} (=V_{DAC} - I_{MON} x R_{DRP}) to regulate the output voltage.

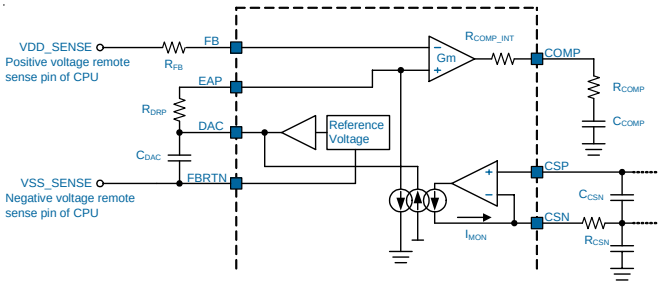


Figure 5. Output Voltage Differential Sense

Total Load Current Sense

The uP9505 uses a low input offset current sense amplifier (CSA) to sense the total load current flowing through inductors for droop function by CSP and CSN (CSPA and CSNA for VDDA) as shown in Figure 6.

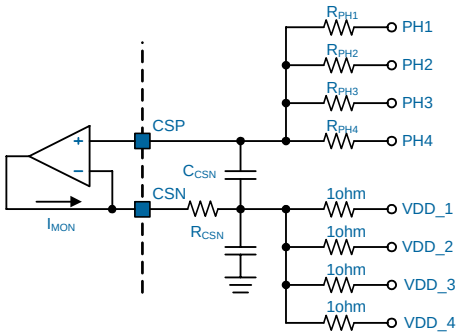


Figure 6.Total Load Current Sense

The voltage across C_{CSN} is proportional to the total load current, and the output current of CSA (I_{MON}) is also proportional to the total load current of the voltage regulator. The sensed current I_{MON} represents the total output current of the regulator, and it is directly used for droop function, total output over current protection, and output current reporting. I_{MON} is calculated as follows.

$$I_{MON} = \frac{I_{OUT} \times \frac{R_{DC}}{P}}{R_{CSN}}$$

In this inductor current sensing topology, R_{PH} and C_{CSN} must be selected according to the equation below:

$$k \times \frac{L}{R_{DC}} = \frac{R_{PH} \times C_{CSN}}{P}$$

where R_{DC} is the DCR of the output inductor L, P is the operation phase number. Theoretically, k should be equal to 1 to sense the instantaneous total load current. But in real application, k is usually between 1.2 to 1.8 for better load transient response. Note that the resistance value of R_{CSN} must be less than 2kΩ to ensure the current sensing circuit in normal operation.

Table 6. VID Table

SVID[7:0]	Voltage(V)	SVID[7:0]	Voltage(V)	SVID[7:0]	Voltage(V)	SVID[7:0]	Voltage(V)
0000_0000	1.55000	0010_0000	1.35000	0100_0000	1.15000	0110_0000	0.95000
0000_0001	1.54375	0010_0001	1.34375	0100_0001	1.14375	0110_0001	0.94375
0000_0010	1.53750	0010_0010	1.33750	0100_0010	1.13750	0110_0010	0.93750
0000_0011	1.53125	0010_0011	1.33125	0100_0011	1.13125	0110_0011	0.93125
0000_0100	1.52500	0010_0100	1.32500	0100_0100	1.12500	0110_0100	0.92500
0000_0101	1.51875	0010_0101	1.31875	0100_0101	1.11875	0110_0101	0.91875
0000_0110	1.51250	0010_0110	1.31250	0100_0110	1.11250	0110_0110	0.91250
0000_0111	1.50625	0010_0111	1.30625	0100_0111	1.10625	0110_0111	0.90625
0000_1000	1.50000	0010_1000	1.30000	0100_1000	1.10000	0110_1000	0.90000
0000_1001	1.49375	0010_1001	1.29375	0100_1001	1.09375	0110_1001	0.89375
0000_1010	1.48750	0010_1010	1.28750	0100_1010	1.08750	0110_1010	0.88750
0000_1011	1.48125	0010_1011	1.28125	0100_1011	1.08125	0110_1011	0.88125
0000_1100	1.47500	0010_1100	1.27500	0100_1100	1.07500	0110_1100	0.87500
0000_1101	1.46875	0010_1101	1.26875	0100_1101	1.06875	0110_1101	0.86875
0000_1110	1.46250	0010_1110	1.26250	0100_1110	1.06250	0110_1110	0.86250
0000_1111	1.45625	0010_1111	1.25625	0100_1111	1.05625	0110_1111	0.85625
0001_0000	1.45000	0011_0000	1.25000	0101_0000	1.05000	0111_0000	0.85000
0001_0001	1.44375	0011_0001	1.24375	0101_0001	1.04375	0111_0001	0.84375
0001_0010	1.43750	0011_0010	1.23750	0101_0010	1.03750	0111_0010	0.83750
0001_0011	1.43125	0011_0011	1.23125	0101_0011	1.03125	0111_0011	0.83125
0001_0100	1.42500	0011_0100	1.22500	0101_0100	1.02500	0111_0100	0.82500
0001_0101	1.41875	0011_0101	1.21875	0101_0101	1.01875	0111_0101	0.81875
0001_0110	1.41250	0011_0110	1.21250	0101_0110	1.01250	0111_0110	0.81250
0001_0111	1.40625	0011_0111	1.20625	0101_0111	1.00625	0111_0111	0.80625
0001_1000	1.40000	0011_1000	1.20000	0101_1000	1.00000	0111_1000	0.80000
0001_1001	1.39375	0011_1001	1.19375	0101_1001	0.99375	0111_1001	0.79375
0001_1010	1.38750	0011_1010	1.18750	0101_1010	0.98750	0111_1010	0.78750
0001_1011	1.38125	0011_1011	1.18125	0101_1011	0.98125	0111_1011	0.78125
0001_1100	1.37500	0011_1100	1.17500	0101_1100	0.97500	0111_1100	0.77500
0001_1101	1.36875	0011_1101	1.16875	0101_1101	0.96875	0111_1101	0.76875
0001_1110	1.36250	0011_1110	1.16250	0101_1110	0.96250	0111_1110	0.76250
0001_1111	1.35625	0011_1111	1.15625	0101_1111	0.95625	0111_1111	0.75625

Functional Description

SVID[7:0]	Voltage(V)	SVID[7:0]	Voltage(V)	SVID[7:0]	Voltage(V)	SVID[7:0]	Voltage(V)
1000_0000	0.75000	1010_0000	0.55000	1100_0000	0.35000	1110_0000	0.15000
1000_0001	0.74375	1010_0001	0.54375	1100_0001	0.34375	1110_0001	0.14375
1000_0010	0.73750	1010_0010	0.53750	1100_0010	0.33750	1110_0010	0.13750
1000_0011	0.73125	1010_0011	0.53125	1100_0011	0.33125	1110_0011	0.13125
1000_0100	0.72500	1010_0100	0.52500	1100_0100	0.32500	1110_0100	0.12500
1000_0101	0.71875	1010_0101	0.51875	1100_0101	0.31875	1110_0101	0.11875
1000_0110	0.71250	1010_0110	0.51250	1100_0110	0.31250	1110_0110	0.11250
1000_0111	0.70625	1010_0111	0.50625	1100_0111	0.30625	1110_0111	0.10625
1000_1000	0.70000	1010_1000	0.50000	1100_1000	0.30000	1110_1000	0.10000
1000_1001	0.69375	1010_1001	0.49375	1100_1001	0.29375	1110_1001	0.09375
1000_1010	0.68750	1010_1010	0.48750	1100_1010	0.28750	1110_1010	0.08750
1000_1011	0.68125	1010_1011	0.48125	1100_1011	0.28125	1110_1011	0.08125
1000_1100	0.67500	1010_1100	0.47500	1100_1100	0.27500	1110_1100	0.07500
1000_1101	0.66875	1010_1101	0.46875	1100_1101	0.26875	1110_1101	0.06875
1000_1110	0.66250	1010_1110	0.46250	1100_1110	0.26250	1110_1110	0.06250
1000_1111	0.65625	1010_1111	0.45625	1100_1111	0.25625	1110_1111	0.05625
1001_0000	0.65000	1011_0000	0.45000	1101_0000	0.25000	1111_0000	0.05000
1001_0001	0.64375	1011_0001	0.44375	1101_0001	0.24375	1111_0001	0.04375
1001_0010	0.63750	1011_0010	0.43750	1101_0010	0.23750	1111_0010	0.03750
1001_0011	0.63125	1011_0011	0.43125	1101_0011	0.23125	1111_0011	0.03125
1001_0100	0.62500	1011_0100	0.42500	1101_0100	0.22500	1111_0100	0.02500
1001_0101	0.61875	1011_0101	0.41875	1101_0101	0.21875	1111_0101	0.01875
1001_0110	0.61250	1011_0110	0.41250	1101_0110	0.21250	1111_0110	0.01250
1001_0111	0.60625	1011_0111	0.40625	1101_0111	0.20625	1111_0111	0.00625
1001_1000	0.60000	1011_1000	0.40000	1101_1000	0.20000	1111_1000	OFF
1001_1001	0.59375	1011_1001	0.39375	1101_1001	0.19375	1111_1001	OFF
1001_1010	0.58750	1011_1010	0.38750	1101_1010	0.18750	1111_1010	OFF
1001_1011	0.58125	1011_1011	0.38125	1101_1011	0.18125	1111_1011	OFF
1001_1100	0.57500	1011_1100	0.37500	1101_1100	0.17500	1111_1100	OFF
1001_1101	0.56875	1011_1101	0.36875	1101_1101	0.16875	1111_1101	OFF
1001_1110	0.56250	1011_1110	0.36250	1101_1110	0.16250	1111_1110	OFF
1001_1111	0.55625	1011_1111	0.35625	1101_1111	0.15625	1111_1111	OFF

Functional Description

Droop (Load Line) Setting

As shown in Figure 5, the current I_{MON} denotes the sensed total load current, which is mirrored to the EAP pin. When load current increases, I_{MON} also increases and creates a voltage drop across R_{DRP}, and makes V_{EAP} lower than the V_{DAC} as follows.

$$V_{EAP} = V_{DAC} - I_{MON} \times R_{DRP} = V_{DAC} - \left(\frac{I_{OUT} \times R_{DC}}{R_{CSN} \times P} \right) \times R_{DRP}$$

where R_{DC} is the DCR of output inductor, P is the operation phase number, and I_{OUT} denotes the total load current. In steady state, the output voltage is regulated to V_{EAP}. As the total load current I_{OUT} increases, I_{MON} increases proportionally, making V_{EAP} decreases accordingly. This makes the output voltage also decreases linearly as the total output current increases, which is also known as active voltage positioning (AVP). The slope of output voltage decrease to total load current increase is referred to as load line. The load line is defined as follows

$$\text{Load Line} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{R_{DC} \times R_{DRP}}{R_{CSN} \times P}$$

Total Output OCP and Operating Phase Number

As shown in Figure 7, the sensed current I_{MON} is mirrored internally and fed to IMON pin (IMONA for VDDA) for total output over current protection (OCP). A resistor R_{IMON} is connected from IMON pin to GND. This current flows through the resistor R_{IMON}, creating voltage drop across it. As the total load current increases, the voltage on IMON pin (V_{IMON}) increases proportionally. When the IMON pin voltage further increases to greater than the OCP threshold (2.56V) for a specific delay time, the total output current protection will be triggered. POK will be pulled low immediately, both UGx and LGx will be held low, and all PWM outputs will in high impedance state to let driver turns off all MOSFETs to shutdown the regulator. The other unaffected voltage regulator will also shut down. The total output OCP is a latch-off type protection, and it can only be reset by VCC5 or EN toggling. The total output OCP delay time can be further programmed by the SMBus register. Avoid adding capacitor to the IMON pin. Additional capacitance to this pin will affect the total output OCP. The default output current level of triggering total output OCP is calculated as follows.

$$I_{OUT\_OCP} = \frac{2.56}{R_{IMON}} \times \frac{P \times R_{CSN}}{R_{DC}}$$

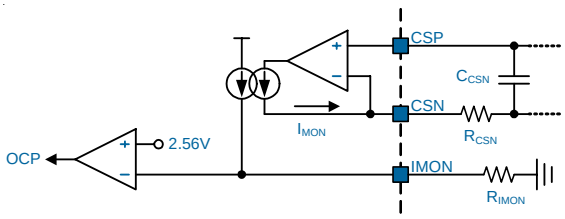


Figure 7. Total Output OCP

The total output OCP level is usually designed for the voltage regulator that is operated in full phase condition by hardware setting. The actual operating phase number is controlled by the SVI2 command or the SMBus Auto Phase setting. When the operating phase number is decreased, the total output OCP level is decreased as well. The total output OCP level is changed per actual operating phase number. Table 7 shows the total output OCP ratio per actual operating phase number and the hardware configuration

Table 7. Total Output OCP and Operating Phase Number

Total Output OCP Ratio		Operating Condition					
		6-Phase	5-Phase	4-Phase	3-Phase	2-Phase	1-Phase
Hardware Configuration	6-Phase	1	10/12	9/12	8/12	5/12	4/12
	5-Phase	--	1	10/12	8/12	5/12	4/12
	4-Phase	--	--	1	9/12	8/12	5/12
	3-Phase	--	--	--	1	9/12	5/12
	2-Phase	--	--	--	--	1	8/12
	1-Phase	--	--	--	--	--	1

Functional Description

Per-Phase Over Current Protection

In addition to the total output current OCP, the controller provides per-phase current OCP to protect the voltage regulator. The controller uses DCR current sensing technique to sense the inductor current in each phase for per-phase over current protection and current balance as shown in Figure 8. In this inductor current sensing topology, the time constant can expressed as follows.

$$k \times \frac{L}{R_{DC}} = R_{CSPx} \times C_{CSx}$$

where L is the output inductor, R_{DC} is its parasitic resistance and k is a constant. Theoretically, if k = 1, the sensed current signal I_{CSNx} can be expressed as follows.

$$I_{CSNx} = \frac{I_{LX} \times R_{DC}}{R_{CSNx}}$$

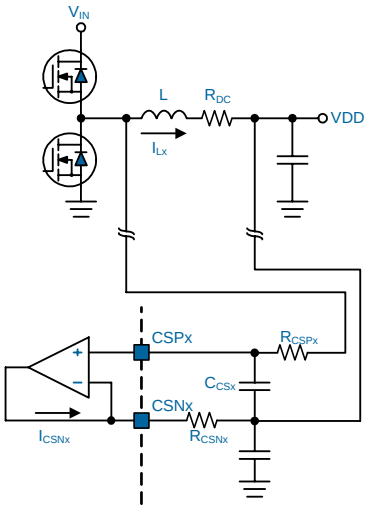


Figure 8. Phase Current Sense

The sensed current I_{CSNx} represents the current in each phase, and it is compared to a current (default = 100uA, SMBus programmable) for per-phase OCP. If the inductor current of any of the active operating phase exceeds the threshold for a specific delay time, the per-phase OCP is triggered. POK will be pulled low immediately, both UGx and LGx will be held low, and all PWM outputs will in high-impedance state to let driver turns off all MOSFETs to shutdown the regulator. The other unaffected voltage regulator will also shut down. The per-phase OCP is a latch-off type protection, and it can only be reset by VCC5 or EN toggling. The per-phase OCP threshold and its delay time can be further programmed by the SMBus register. Note that the resistance value of R_{CSNx} must be less than 2kΩ to ensure the current sensing circuit in normal operation. The resistance of R_{CSNx} and the default per-phase OCP level can be obtained using equation as follows:

$$R_{CSNx} = \frac{I_{OCP\_perphase} \times R_{DC}}{100uA}$$

Over Voltage Protection (OVP)

The controller monitors the voltage on FB pin (FBA for VDDA) for over voltage protection. After output voltage ramps up to Vboot, the controller initiates OVP function. Once V_{FB} exceeds V_{EAP} + OVP threshold for a specific delay time, OVP is triggered. POK will be pulled low immediately, UGx will be held low, LGx will be held high, and PWM outputs will be low to let driver turns on low side MOSFET and turns off high side MOSFET to protect CPU. Since the low side MOSFET is turned on, the regulator output capacitor will be discharged and output voltage decreases as well. When FB pin voltage decreases to lower than typical 0.5V, LGx will be held low (PWM outputs turns to high impedance state) to turn off the low side MOSFET to avoid negative output voltage. The other unaffected voltage regulator will also shut down. The OVP is a latch-off type protection, and it can only be reset by VCC5 or EN toggling. The OVP detection circuit has a fixed delay time to prevent false trigger. The OVP threshold can be further programmed by the SMBus register.

Under Voltage Protection (UVP)

The controller monitors the voltage on FB pin (FBA for VDDA) for under voltage protection. After output voltage ramps up to Vboot, the controller initiates UVP function. Once V_{FB} is lower than V_{EAP} - UVP threshold for a specific delay time, UVP is triggered. POK will be pulled low immediately, both UGx and LGx will be held low, and all PWM outputs will in high-impedance state to let driver turns off all MOSFETs to shutdown the regulator. The other unaffected voltage regulator will also shut down. The UVP is a latch-off type protection, and it can only be reset by VCC5 or EN toggling. The UVP detection circuit has a fixed delay time to prevent false trigger. The UVP threshold can be further programmed by the SMBus register.

Thermal Monitoring and VRHOT#

The TSEN pin (TSENA for VDDA) is used for voltage regulator thermal monitoring. Connect a negative temperature coefficient (NTC) thermistor network to this pin for sensing VR temperature. The curve of TSEN (TSENA for VDDA) pin voltage and the sensed temperature is shown in Figure 9. The NTC thermistor is placed close to the hottest point of the regulator, normally close to the inductor and low-side MOSFET of phase 1. The controller asserts VRHOT# when the sensed temperature is higher than the value of SMBus register 0x29h (TEMP_VRHOT), in which the default value is 05h (106°C). Either VDD or VDDA regulator can trigger the VRHOT# as long as the temperature of any of the two regulators exceeds the maximum temperature threshold. The threshold of VRHOT# assertion can be further programmed by SMBus register. The recommended NTC thermistor is 10kΩ/β = 3380 by Murata (NCP18XH103F03RB) and the recommended lower dividing resistor is 6kΩ.

Functional Description

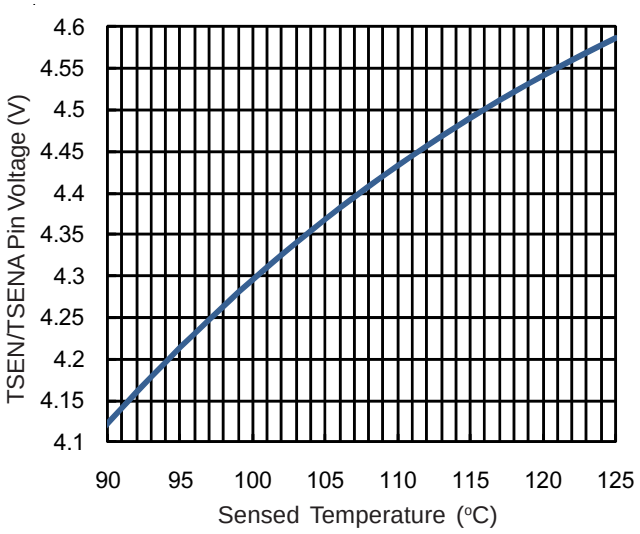


Figure 9. TSEN/TSENA Pin Voltage and Sensed Temperature

Power OK Indication

The uP9505 has a power ok indication pin for VDD/VDDA controllers. The VDD/VDDA controller monitors DAC/DACA voltage for power ok indication. When DAC/DACA voltage ramps to the target output voltage, the controller asserts POK. The POK is pulled low immediately if any of the faults (OCP, OVP and UVP) occurs.

Control Loop

The uP9505 adopts the uPI proprietary RCOT+™ control technology. The RCOT uses the constant on-time modulator. The output voltage is sensed to compare with the internal high accurate reference voltage. The reference voltage is commanded by CPU through the SVI2 interface or by system through SMBus interface. The amplified error signal V_{COMP} is compared to the internal ramp to initiate a PWM on-time. The RCOT+™ features easy design, fast transient response and is smooth mode transition and especially suitable for powering the microprocessor

Serial VID Interface 2.0 (SVI2)

Serial VID Interface 2.0 (SVI2) is a three wire (SVC, SVD and SVT) serial synchronous interface defined by AMD to transfer power management information between the CPU and the VR controller. The SVI2 bus operates at a maximum frequency of 21MHz. CPU is always the master, and the VR controller is always the slave. SVC, SVD and SVT pins are both in push-pull structure. SVC is source synchronous clock signal from the CPU. Only PWROK is asserted, SVC and SVD can be used to serially transmit data from the CPU to VR.

SMBus Interface

The uP9505 features an SMBus interface and data registers to allow user to adjust various platform operating parameters for VDD and VDDA. The supported operating parameters that can be adjusted through the SMBus are summarized as Table 8. The main function is to dynamically change the offset voltage, switching frequency, operating phase number, and load line according to the total load current. This function is referred to as Auto Phase, and it provides user the maximal flexibility in the platform design to maximize voltage regulator's efficiency and the processor performance as well. For the 4-phase VDD regulator, there are four load current states (LCS) to set. The switching frequency, offset voltage, operating phase number and load line in each LCS can be programmed independently. For the 2-phase VDDA regulator, there are two load current states (LCS) to set. The switching frequency, offset voltage and operating phase number in each LCS can also be programmed independently.

VM0~ VM4 (AVM0 for VDDA): Define the thresholds for six load current states (LCS0~LCS5) for VDD. The VDD controller converts IMON pin voltage V_{IMON} to a digital content, which represents the total output current. The VMx setting is defined as the ratio of IMON pin voltage to 2.56V

(2.56V denotes when VDD output current reaches its summed total current). It takes 2.56V as the full scale, and 6-bits means that there are 64 steps for user to choose from. Each load current state register has 6-bits to set the level of output current that the load current state is entered. The controller compares the VMx content and the I_{MON} (refer to the section of **Total Output Over Current Protection**) to determine which load current state should be entered and executes the corresponding operating parameter settings (frequency, offset and operating phase number).

LCS0: V_{IMON} > VM0, highest load current state

LCS1: VM0 > V_{IMON} > VM1

LCS2: VM1 > V_{IMON} > VM2

LCS3: VM2 > V_{IMON} > VM3

LCS4: VM3 > V_{IMON} > VM4

LCS5: VM4 > V_{IMON}, lowest load current state.

VM0_Hys~ VM4_Hys (AVM0_Hys for VDDA):

Define the hysteresis of VM0~VM4. The hysteresis is also defined as the ratio of IMON pin voltage to 2.56V.

VOFS0~VOFS5 (AVOFS0, AVOFS1 for VDDA):

Define the offset voltage in each load current state. 8-bits content setting with 6.25mV/step.

IICF0~ IICF5 (AIICF0, AIICF1 for VDDA):

Define the switching frequency in each load current state. The switching frequency is defined as the ratio to current setting per R_{TONSET} and V_{IN}. The default is 1000 for 100%. 0000 = 60%; 0001 = 65%; 0010 = 70%;0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100%; 1001=125%; 1010 = 150%; 1011 = 175%; 1100 = 200%; 1101 = 225%; 1110 = 250%; 1111 = 275%.

IICP0~IICP5 (AIICP0, AIICP1 for VDDA):

Define the operating phase number in each load current state. The operating phase number can be full-phase to single phase

IICLL0~ IICLL5 (AIICLL0, AIICLL1 for VDDA):

Define the load line value in each load current state. The load line adjustment is defined as the ratio to current droop setting. The default is 0110 for 100%. 0000 = 0%; 0001 = 40%; 0010 = 60%;0011 = 70%; 0100 = 80%; 0101 = 90%; 0110 = 100%; 0111 =110%; 1000 = 120%;1001=130%; 1010 = 140%; 1011 = 150%; 1100 = 160%; 1101 =170%; 1110 = 180%; 1111 = 190%.

RCOMP1, RCOMP2 (ARCOMP1, ARCOMP2 for VDDA): Define the compensation resistor value. The compensation resistor value for the regulator operating in single-phase operation and multi-phase operation can be adjusted separately.

GCOMP (AGCOMP for VDDA):

For OTA transconductance setting for voltage control loop. It is defined as the ratio to the default value of 2020 uA/V.

OC/UV/OV:

OC/UV/OV is used for the threshold adjustment of per-phase OCP, UVP and OVP, respectively.

OCP Delay: For total OCP threshold and per-phase OCP delay time setting.

LCHVID (ALCHVID for VDDA):

This register stores the 8-bits VID code. When latch VID function is enabled, controller will ignore the SetVID command from CPU and move output voltage to the targeted value.

IMON (IMONA for VDDA):

The register reports real IMON value (FFh when V_{IMON} = 2.56V).

VFB (VFBA for VDDA):

This register reports the output voltage that is converted by the internal ADC with 6.25mV/LSB.

Table 8. SMBus Configuration Register

Reg. Addr.	Focus Rail	Reg. Name	Access	Default	Description
0x01	VDD	VM0[7:2]	R/W	00h	Set internal IMON voltage level 0 VIMON > Level 0 => LCS0 (highest current state) Bit[1:0] : Don't care VM0 = (Bit[7:2]/64) x 2.56 VM0 setting is defined as the ratio to IMON voltage to 2.56V
0x02	VDD	VM1[7:2]	R/W	00h	Set internal IMON voltage level 1 VIMON > Level 1 => LCS1 VIMON < Level 1 => LCS2 Bit[1:0] : Don't care VM1 = (Bit[7:2]/64) x 2.56 VM1 setting is defined as the ratio to IMON voltage to 2.56V
0x03	VDD	VM2[7:2]	R/W	00h	Set internal IMON voltage level 2 VIMON > Level 2 => LCS2 VIMON < Level 2 => LCS3 Bit[1:0] : Don't care VM2 = (Bit[7:2]/64) x 2.56 VM2 setting is defined as the ratio to IMON voltage to 2.56V
0x04	VDD	VM3[7:2]	R/W	00h	Set internal IMON voltage level 3 VIMON > Level 3 => LCS3 VIMON < Level 3 => LCS4 Bit[1:0] : Don't care VM3 = (Bit[7:2]/64) x 2.56 VM3 setting is defined as the ratio to IMON voltage to 2.56V
0x05	VDD	VM4[7:2]	R/W	00h	Set internal IMON voltage level 4 VIMON > Level 4 => LCS4 VIMON < Level 4 => LCS5 Bit[1:0] : Don't care VM4 = (Bit[7:2]/64) x 2.56 VM4 setting is defined as the ratio to IMON voltage to 2.56V
0x06	VDD	VM0_Hys[6:4] VM1_Hys[2:0]	R/W	00h	VBit[7]: Don't care Bit[6:4] : Set VM0 Hysteresis, 8 steps Hys = (2.56 / 100) x (2 + bit[6:4]) Bit[3]: Don't care Bit[2:0] : Set VM1 Hysteresis, 8 steps Hys = (2.56 / 100) x (2 + bit[2:0]) Hysteresis is defined as the ratio of IMON pin voltage to 2.56V
0x07	VDD VDDA	VM2_Hys[6:4] AVM0_Hys[2:0]	R/W	00h	Bit[7]: Don't care Bit[6:4] : Set VM2 Hysteresis, 8 steps Hys = (2.56 / 100) x (2 + bit[6:4]) Bit[3]: Don't care Bit[2:0] : Set AVM0 Hysteresis, 8 steps Hys= (2.56 / 100) x (2+bit[2:0]) Hysteresis is defined as the ratio of IMON pin voltage to 2.56V
0x08	VDD	VM3_Hys[6:4] VM4_Hys[2:0]	R/W	00h	Bit[7]: Don't care Bit[6:4] : Set VM3 Hysteresis, 8 steps Hys = (2.56 / 100) x (2 + bit[6:4]) Bit[3]: Don't care Bit[2:0] : Set VM4 Hysteresis, 8 steps Hys = (2.56 / 100) x (2 + bit[2:0]) Hysteresis is defined as the ratio of IMON pin voltage to 2.56V

Reg. Addr.	Focus Rail	Reg. Name	Access	Default	Description
0x09	VDD	IICP0[6:4] IICP1[2:0]	R/W	66h	VDD Operation Phase Number Setting Bit[6:4] : Phase Number of VDD LCS0 Bit[2:0] : Phase Number of VDD LCS1 110 : 6 Phase; 101 : 5 Phase; 100 : 4 Phase; 011 : 3 Phase; 010 : 2 Phase; 001 : 1 Phase CCM; 000 : 1 Phase PSM
0x0A	VDD	IICP2[6:4] IICP3[2:0]	R/W	66h	VDD Operation Phase Number Setting Bit[6:4] : Phase Number of VDD LCS2 Bit[2:0] : Phase Number of VDD LCS3 110 : 6 Phase; 101 : 5 Phase; 100 : 4 Phase; 011 : 3 Phase; 010 : 2 Phase; 001 : 1 Phase CCM; 000 : 1 Phase PSM
0x0B	VDD	IICP4[6:4] IICP5[2:0]	R/W	66h	VDD Operation Phase Number Setting Bit[6:4] : Phase Number of VDD LCS4 Bit[2:0] : Phase Number of VDD LCS5 110 : 6 Phase; 101 : 5 Phase; 100 : 4 Phase; 011 : 3 Phase; 010 : 2 Phase; 001 : 1 Phase CCM; 000 : 1 Phase PSM
0x0C	VDD	VOFS0[7:0]	R/W	00h	Voltage offset of VDD LCS0. (6.25mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset Upper and lower limits = +/-750mV 00000000 = +0mV 00000001 = +6.25mV 00111100 = +375mV 01111000 = +750mV 01111111 = +750mV 10000000 = -0mV 10000001 = -6.25mV 10111100 = -375mV 11111000 = -750mV 11111111 = -750mV
0x0D	VDD	VOFS1[7:0]	R/W	00h	Voltage offset of VDD LCS1. (6.25mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset Upper and lower limits = +/-750mV 00000000 = +0mV 00000001 = +6.25mV 00111100 = +375mV 01111000 = +750mV 01111111 = +750mV 10000000 = -0mV 10000001 = -6.25mV 10111100 = -375mV 11111000 = -750mV 11111111 = -750mV
0x0E	VDD	VOFS2[7:0]	R/W	00h	Voltage offset of VDD LCS2. (6.25mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset Upper and lower limits = +/-750mV 00000000 = +0mV 00000001 = +6.25mV 00111100 = +375mV 01111000 = +750mV 01111111 = +750mV 10000000 = -0mV 10000001 = -6.25mV 10111100 = -375mV 11111000 = -750mV 11111111 = -750mV

Reg. Addr.	Focus Rail	Reg. Name	Access	Default	Description
0x0F	VDD	VOFS3[7:0]	R/W	00h	Voltage offset of VDD LCS3. (6.25mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset Upper and lower limits = +/-750mV 00000000 = +0mV 00000001 = +6.25mV 00111100 = +375mV 01111000 = +750mV 01111111 = +750mV 10000000 = -0mV 10000001 = -6.25mV 10111100 = -375mV 11111000 = -750mV 11111111 = -750mV
0x10	VDD	VOFS4[7:0]	R/W	00h	Voltage offset of VDD LCS4. (6.25mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset Upper and lower limits = +/-750mV 00000000 = +0mV 00000001 = +6.25mV 00111100 = +375mV 01111000 = +750mV 01111111 = +750mV 10000000 = -0mV 10000001 = -6.25mV 10111100 = -375mV 11111000 = -750mV 11111111 = -750mV
0x11	VDD	VOFS5[7:0]	R/W	00h	Voltage offset of VDD LCS5. (6.25mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset Upper and lower limits = +/-750mV 00000000 = +0mV 00000001 = +6.25mV 00111100 = +375mV 01111000 = +750mV 01111111 = +750mV 10000000 = -0mV 10000001 = -6.25mV 10111100 = -375mV 11111000 = -750mV 11111111 = -750mV
0x12	VDD	IICF0[7:4] IICF1[3:0]	R/W	88h	VDD Operation Frequency Setting Bit[7:4] : Phase Number of VDD LCS0, default = 100% Bit[3:0] : Phase Number of VDD LCS1, default = 100% 0000 = 60%; 0001 = 65%; 0010 = 70%;0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100%(default); 1001=125%; 1010 = 150%; 011 = 175%; 1100 = 200%; 1101 = 225%; 1110 = 250%; 1111 = 275%
0x13	VDD	IICF2[7:4] IICF3[3:0]	R/W	88h	VDD Operation Frequency Setting Bit[7:4] : Phase Number of VDD LCS2, default = 100% Bit[3:0] : Phase Number of VDD LCS3, default = 100% 0000 = 60%; 0001 = 65%; 0010 = 70%;0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100%(default); 1001=125%; 1010 = 150%; 011 = 175%; 1100 = 200%; 1101 = 225%; 1110 = 250%; 1111 = 275%

Reg. Addr.	Focus Rail	Reg. Name	Access	Default	Description
0x14	VDD	IICF4[7:4] IICF5[3:0]	R/W	88h	VDD Operation Frequency Setting Bit[7:4] : Phase Number of VDD LCS4, default = 100% Bit[3:0] : Phase Number of VDD LCS5, default = 100% 0000 = 60%; 0001 = 65%; 0010 = 70%;0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100%(default); 1001=125%; 1010 = 150%; 011 = 175%; 1100 = 200%; 1101 = 225%; 1110 = 250%; 1111 = 275%
0x15	VDD	IICLL0[7:4] IICLL1[3:0]	R/W	66h	VDD Load Line Setting Bit[7:4] : Load line setting of VDD LCS0, default = 100% Bit[3:0] : Load line setting of VDD LCS1, default = 100% 0000 = 0%; 0001 = 40%; 0010 = 60%; 0011 = 70%; 0100 = 80%; 0101 = 90%; 0110 = 100%(default); 0111 =110%; 1000 = 120%; 1001 =130%; 1010 = 140%; 1011 = 150%; 1100 = 160%; 1101 =170%; 1110 = 180%; 1111 = 190%
0x16	VDD	IICLL2[7:4] IICLL3[3:0]	R/W	66h	VDD Load Line Setting Bit[7:4] : Load line setting of VDD LCS2, default = 100% Bit[3:0] : Load line setting of VDD LCS3, default = 100% 0000 = 0%; 0001 = 40%; 0010 = 60%; 0011 = 70%; 0100 = 80%; 0101 = 90%; 0110 = 100%(default); 0111 =110%; 1000 = 120%; 1001 =130%; 1010 = 140%; 1011 = 150%; 1100 = 160%; 1101 =170%; 1110 = 180%; 1111 = 190%
0x17	VDD	IICLL4[7:4] IICLL5[3:0]	R/W	66h	VDD Load Line Setting Bit[7:4] : Load line setting of VDD LCS4, default = 100% Bit[3:0] : Load line setting of VDD LCS5, default = 100% 0000 = 0%; 0001 = 40%; 0010 = 60%; 0011 = 70%; 0100 = 80%; 0101 = 90%; 0110 = 100%(default); 0111 =110%; 1000 = 120%; 1001 =130%; 1010 = 140%; 1011 = 150%; 1100 = 160%; 1101 =170%; 1110 = 180%; 1111 = 190%
0x18	VDD	CB_EN[7] PH1_IGAIN[6:4] PH2_IGAIN[2:0]	R/W	44h	Bit[7]: On/Off control of VDD current balance function, default = ON, "0" = ON, "1" = OFF Bit[6:4] : VDD Phase 1 current balance gain adjust, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5% Bit[3] : Don't care Bit[2:0] : VDD Phase 2 current balance gain adjust, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5%
0x19	VDD	PH3_IGAIN[6:4] PH4_IGAIN[2:0]	R/W	44h	Bit[7] : Don't care Bit[6:4] : VDD Phase 3 current balance gain adjust, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default) ; 101 = 112.5%; 110 = 125%; 111 = 137.5% Bit[3] : Don't care Bit[2:0] : VDD Phase 4 current balance gain adjust, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5%
0x1B	VDD	PH1_IOS[6:4] PH2_IOS[2:0]	R/W	00h	Bit[7]: Don't care Bit[6:4] : VDD Phase 1 current balance offset, default = 0uA 000 = 0uA(default); 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA Bit[3]: Don't care Bit[2:0] : VDD Phase 2 current balance offset, default = 0uA 000 = 0uA(default); 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA

Reg. Addr.	Focus Rail	Reg. Name	Access	Default	Description
0x1C	VDD	PH3_IOS[6:4] PH4_IOS[2:0]	R/W	00h	Bit[7]: Don't care Bit[6:4] : VDD Phase 3 current balance offset, default = 0uA 000 = 0uA(default); 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA Bit[3]: Don't care Bit[2:0] : VDD Phase 4 current balance offset, default = 0uA 000 = 0uA(default); 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA
0x1E	VDD	RCOMP1[7:4] RCOMP2[3:0]	R/W	73h	RCOMP Resistor Setting Bit[7:4] : Single-phase operation RCOMP RCOMP = 2.5K x (1+[7:4]), default = 20K Bit[3:0] : Multi-phase operation RCOMP RCOMP = 2.5K x (1+[3:0]), default = 10K
0x1F	VDD	GCOMP[3:0]	R/W	80h	VDD OTA Gm value selection GCOMP[3] : VDD OTA Gm value selection 0 = force to use default value (2020uA/V), GCOMP[2:0] setting will be ignored(default); 1 = use the value set in GCOMP[2:0] GCOMP[2:0] : VDD transconductance Gm setting, applied to all operating phase number, defined as the ratio to default (=2020uA/V) 000 = 1X(default); 001 = 1.17X; 010 = 1.31X; 011 = 1.45X; 100 = 1.69X; 101 = 0.81X; 110 = 0.6X; 111 = 0.33X
0x20	VDD	LCHVID[7:0]	R/W	48h	VDD Latch VID Register. Default = 48h = 1.1V
0x21	VDD	IMON[7:0]	RO	--	VDD IMON reporting
0x22	VDD	VFB[7:0]	RO	--	VDD voltage Reading Voltage reading values in VFB[7:0] is from A/D result of actual output voltage by default.
0x23	VDD	Protect_Ind[6:0]	RO	00h	VDD protection indicator, indicating which protection is triggered Bit[7] : Don't care Bit[6] : OVP Indicator "0" = Not Active, "1" = Active Bit[5] : UVP Indicator "0" = Not Active, "1" = Active Bit[4] : OCP Indicator "0" = Not Active, "1" = Active Bit[3] : Per Phase OCP Indicator "0" = Not Active, "1" = Active Bit[2:0]: Per Phase OCP Indicator if Bit[3]=1 001 = PH1; 010 = PH2; 011 = PH3 100 = PH4; 101 = PH5; 110 = PH6 Report value of Bit[2:0] is valid only when Bit[3]=1
0x24	shared	OCP Delay [6:0]	R/W	32h	Both VDD and VDDA share the same setting Bit[7] : Don't care Bit[6:4] : Total OCP Delay Time 000 = 5us; 001 = 10us; 010 = 15us; 011 = 20us(default); 100 = 25us; 101 = 30us; 110 = 35us; 111 = 40us Bit[3] : Don't care Bit[2:0] : Per Phase OCP Delay Time 000 = 2us; 001 = 4us; 010 = 6us(default) ; 011 = 8us; 100 = 10us; 101 = 12us; 110 = 14us; 111 = 16us

Reg. Addr.	Focus Rail	Reg. Name	Access	Default	Description
0x25	shared	OC/UV/OV [5:0]	R/W	00h	Both VDD and VDDA share the same setting Bit[7] : Don't care Bit[5:4] : Per Phase OCP Current 00 = 100uA(default); 01 = 120uA; 10 = 140uA; 11 = 160uA Bit[3:2] : UVP Threshold 00 = 325mV(default); 01 = 405mV; 10 = 485mV; 11 = 570mV Bit[1:0] : OVP Threshold 00 = 325mV(default); 01 = 405mV; 10 = 485mV; 11 = 570mV
0x26	shared	AVR_SR[6:4] VR_SR[2:0]	R/W	22h	Bit[7] : Don't care Bit [6:4] : VDD d-VID upward slew rate selection Bit [2:0] : VDDA d-VID upward slew rate selection DVID upward slew rate selection. Setting range from 8 to 22 mV/uS. Total 7 steps and 2mV/us per-LSB. Default is 12mV/us. 000 = 8mV/us; 001 = 10mV/us; 010 = 12mV/us(default); 011 = 14mV/us; 100 = 16mV/us; 101 = 18mV/us; 110 = 20mV/us; 111 = 22mV/us;
0x27	VDD	Misc1[7:0]	R/W	0Fh	Bit[7] :OFS control 2 Report value of Bit[7] is valid only when Bit[4]=1 "0" =Only SMBus, "1" = SVI2+ SMBus Bit[6] : VDAC Control "0" = Follow SVI2, "1" = Ignore SVI2 Bit[5] : PWR State Control "0" = Follow SVI2, "1" = Ignore SVI2 Bit[4]: OFS control1 "0" = Follow SVI2, "1" = Follow Bit[7] Bit[3]: Total OCP Control "0" = Disable, "1" = Enable(default) Bit[2]: Per-phase OCP Control "0" = Disable, "1" = Enable(default) Bit[1]: OVP Control "0" = Disable, "1" = Enable(default) Bit[0]: UVP Control "0" = Disable, "1" = Enable(default)
0x28	VDD	Misc2[7:0]	R/W	04h	Bit[7] : Load Line Control "0" = Follow SVI2 "1" = Ignore SVI2 Bit[6] : Spread Spectrum for switching frequency "0" = Disable Spread Spectrum(default) "1" = Enable Spread Spectrum Bit[5]: Selection of the data source of SMBus Reg. 0x22h VDD output voltage reading(VFB [7:0]) "0" = From A/D(default) "1" = From SVI2 Bit[4] : Auto Phase Enable Control "0" = Disable Auto Phase(default) "1" = Enable Auto Phase Bit[3] : Load Line Enable Control "0" = Enable Load Line(default) "1" = Disable Load Line (LL = 0) Bit[2] : PSM Enable Control "0" = Disable PSM "1" = Enable PSM(default) Bit[1:] : USM Enable Control "0" = Disable USM(default) "1" = Enable USM

Reg. Addr.	Focus Rail	Reg. Name	Access	Default	Description
0x29	VDD, shared	OTPEN1[7] OTPEN2[6] TEMP_VRHOT [4:0]	R/W	45h	Bit[7] : OTP Shutdown Enable Control (TSEN/TSENA) "0" = Disable(default), "1" = Enable Bit[6] : OTP(internal) Enable Control (controller thermal shutdown) "0"= Disable, "1" = Enable(default) Bit[5] : Don't care Bit[4] : VRHOT# Enable Control "0" = Enable(default), "1" = Disable Bit[3:0] : Shift left by LSB, Temp range from 91°C to 121°C, default = 106°C, 3°C/LSB 0000 = No Shift; 0001 = Shift 1LSB; 0010 = Shift 2LSB; 0011 = Shift 3LSB; 0100 = Shift 4LSB; 0101 = Shift 5LSB (default) ; 0110 = Shift 6LSB; 0111 = Shift 7LSB; 1000 = Shift 8LSB; 1001 = Shift 9LSB; 1010 = Shift 10LSB
0x2A	shared	WD[7:5] SVC_Timeout [2:0]	R/W	05h	Watchdog Timer Bit[7] : "1" = Enable ; "0" = Disable(default) Bit[6] : Watchdog status "0" = SMBus transactions occurred within watchdog period "1" = time between SMBus transaction exceeds watchdog period When the watchdog function is enabled, if no SMBus transactions occur within a selected period (600ms or 1200ms), all register contents will be reset to default value. This bit is cleared by SMBus read from this register. Bit[5] : Watchdog period "0" = 600ms(default) "1" = 1200ms SVC_Timeout: Bit[2:0] : 000 = 0.5us; 001 = 1us; 010 = 2us; ... ; 110 = 32us; 111 = 64us
0x2E	VDD	Ramp_COMP [7:0]	R/W	88h	Ramp_COMP[7:4] is for multi-phase operation, default = 100% 0000=60%; 0001=65%; 0010=70%; 0011=75%; 0100=80%; 0101=85%; 0110=90%; 0111=95%; 1000=100%(default); 1001=105%; 1010=110%; 1011=115%; 1100=120%; 1101=125%; 1110=130%; 1111=135% Ramp_COMP[3:0] is for single-phase operation, default = 100% 0000=60%; 0001=65%; 0010=70%; 0011=75%; 0100=80%; 0101=85%; 0110=90%; 0111=95%; 1000=100%(default); 1001=105%; 1010=110%; 1011=115%; 1100=120%; 1101=125%; 1110=130%; 1111=135%
0x2F	VDD	TM[7:0]	R/W	--	VDD SMBus Thermal Monitor Value Reading. This register stores the value of A/D conversion for TSEN pin
0x30	VDDA	AllCP0[3:2] AllCP1[1:0]	R/W	05h	VDDA Operation Phase Number Setting Bit[3:2] : Phase Number of VDDA LCS0 Bit[1:0] : Phase Number of VDDA LCS1 01: 2 Phase; 00: 1 Phase
0x31	VDDA	AVOFS0[7:0]	R/W	00h	Voltage offset of VDDA LCS0. (6.25mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset Upper and lower limits = +/-750mV 00000000 = +0mV 00000001 = +6.25mV 00111100 = +375mV 01111000 = +750mV 01111111 = +750mV 10000000 = -0mV 10000001 = -6.25mV 10111100 = -375mV 11111000 = -750mV 11111111 = -750mV

Reg. Addr.	Focus Rail	Reg. Name	Access	Default	Description
0x32	VDDA	AVOFS1[7:0]	R/W	00h	Voltage offset of VDDA LCS1. (6.25mV / step) Bit7 is sign bit, "0"=positive offset; "1"=negative offset Upper and lower limits = +/-750mV 00000000 = +0mV 00000001 = +6.25mV 00111100 = +375mV 01111000 = +750mV 01111111 = +750mV 10000000 = -0mV 10000001 = -6.25mV 10111100 = -375mV 11111000 = -750mV 11111111 = -750mV
0x33	VDDA	AllCF0[3:2] AllCF1[1:0]	R/W	88h	VDDA Operation Frequency Setting Bit[7:4] : Phase Number of VDDA LCS0, default = 100% Bit[3:0] : Phase Number of VDDA LCS1, default = 100% 0000 = 60%; 0001 = 65%; 0010 = 70%;0011 = 75%; 0100 = 80%; 0101 = 85%; 0110 = 90%; 0111 = 95%; 1000 = 100%(default); 1001=125%; 1010 = 150%; 1011 = 175%; 1100 = 200%; 1101 = 225%; 1110 = 250%; 1111 = 275%
0x34	VDDA	AllCLL0[3:2] AllCLL1[1:0]	R/W	66h	VDDA Load Line Setting Bit[7:4] : Load line setting of VDDA LCS0, default = 100% Bit[3:0] : Load line setting of VDDA LCS1, default = 100% 0000 = 0%; 0001 = 40%; 0010 = 60%;0011 = 70%; 0100 = 80%; 0101 = 90%; 0110 = 100%(default); 0111 =110%; 1000 = 120%; 1001=130%; 1010 = 140%; 1011 = 150%; 1100 = 160%; 1101 =170%; 1110 = 180%; 1111 = 190%
0x35	VDDA	ACB_EN[7] APH1_IGAIN [6:4] APH2_IGAIN [2:0]	R/W	44h	Bit[7]: On/Off control of VDDA current balance function, default = ON, "0" = ON, "1" = OFF Bit[6:4] : VDDA Phase 1 current balance gain adjust, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5% Bit[3] : Don't care Bit[2:0] : VDDA Phase 2 current balance gain adjust, default = 100% 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100% (default); 101 = 112.5%; 110 = 125%; 111 = 137.5%
0x36	VDDA	APH1_IOS[6:4] APH2_IOS[2:0]	R/W	00h	Bit[7]: Don't care Bit[6:4] : VDDA Phase 1 current balance offset, default = 0uA 000 = 0uA(default); 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA Bit[3]: Don't care Bit[2:0] : VDDA Phase 2 current balance offset, default = 0uA 000 = 0uA(default); 001 = 2uA; 010 = 4uA; 011 = 6uA; 100 = 8uA; 101 = 10uA; 110 = 12uA; 111 = 14uA
0x37	VDDA	ARCOMP1[7:4] ARCOMP2[3:0]	R/W	73h	ARCOMP Resistor Setting Bit[7:4]: single-phase operation ARCOMP ARCOMP = 2.5K x (1+[7:4]), default = 20K Bit[3:0]: multi-phase operation ARCOMP ARCOMP = 2.5K x (1+[3:0]), default = 10K

Reg. Addr.	Focus Rail	Reg. Name	Access	Default	Description
0x38	VDDA	AGCOMP[3:0]	R/W	00h	VDDA OTA Gm value selection AGCOMP[3] : VDDA OTA Gm value selection 0 = force to use default value (2020uA/V), AGCOMP[2:0] setting will be ignored(default); 1 = use the value set in AGCOMP[2:0] AGCOMP[2:0] : VDDA transconductance Gm setting, applied to all operating phase number, defined as the ratio to default (=2020uA/V) 000 = 1X(default); 001 = 1.17X; 010 = 1.31X; 011 = 1.45X; 100 = 1.69X; 101 = 0.81X; 110 = 0.6X;111 = 0.33X
0x39	VDDA	ARamp_COMP [7:0]	R/W	88h	ARamp_COMP[7:4] is for multi-phase operation, default = 100% 0000=60%; 0001=65%; 0010=70%; 0011=75%; 0100=80%; 0101=85%; 0110=90%; 0111=95%; 1000=100%(default); 1001=105%; 1010=110%; 1011=115%; 1100=120%; 1101=125%; 1110=130%; 1111=135% ARamp_COMP[3:0] is for single-phase operation, default = 100% 0000=60%; 0001=65%; 0010=70%; 0011=75%; 0100=80%; 0101=85%; 0110=90%; 0111=95%; 1000=100%(default); 1001=105%; 1010=110%; 1011=115%; 1100=120%; 1101=125%; 1110=130%; 1111=135%
0x3A	VDDA	IMONA[7:0]	RO	--	VDDA IMONA reporting
0x3B	VDDA	VFBA[7:0]	RO	--	VDDA Voltage Reading Voltage reading values in VFBA[7:0] is from A/D result of actual output voltage by default.
0x3C	VDDA	AMisc1[7:0]	R/W	0Fh	Bit[7] :OFS control 2 Report value of Bit[7] is valid only when Bit[4]=1 "0" =Only SMBus , "1" = SVI2+ SMBus Bit[6] : VDAC Control "0" = Follow SVI2, "1" = Ignore SVI2 Bit[5] : PWR State Control "0" = Follow SVI2, "1" = Ignore SVI2 Bit[4]: OFS control1 "0" = Follow SVI2, "1" = Follow Bit[7] Bit[3]: Total OCP Control "0" = Disable, "1" = Enable(default) Bit[2]: Per-phase OCP Control "0" = Disable, "1" = Enable(default) Bit[1]: OVP Control "0" = Disable, "1" = Enable(default) Bit[0]: UVP Control "0" = Disable, "1" = Enable(default)

Reg. Addr.	Focus Rail	Reg. Name	Access	Default	Description
0x3D	VDDA	AMisc2[7:0]	R/W	04h	Bit[7] : Load Line Control "0" = Follow SVI2, "1" = Ignore SVI2 Bit[6] : Spread Spectrum for switching frequency "0" = Disable Spread Spectrum(default) "1" = Enable Spread Spectrum Bit[5]: Selection of the data source of SMBus Reg. 0x3Bh VDDA output voltage reading(VFBA[7:0]) "0" = From AD (default) "1" = From SVI2 Bit[4] : Auto Phase Enable Control "0" = Disable Auto Phase(default) "1" = Enable Auto Phase Bit[3] : Load Line Enable Control "0" = Enable Load Line(default) "1" = Disable Load Line (LL = 0) Bit[2] : PSM Enable Control "0" = Disable PSM "1" = Enable PSM(default) Bit[1:] : USM Enable Control "0" = Disable USM(default) "1" = Enable USM
0x3E	VDDA	ATEMP_VRH-OT [4:0]	R/W	05h	Bit[7] : Don't care Bit[6] : Don't care Bit[5] : Don't care Bit[4] : VRHOT# Enable Control 0" = Enable(default), "1" = Disable Bit[3:0] : Shift left by LSB, Temp range from 91°C to 121°C default = 106°C, 3°C/LSB 0000 = No Shift; 0001 = Shift 1LSB; 0010 = Shift 2LSB; 0011 = Shift 3LSB; 0100 = Shift 4LSB;0101 = Shift 5LSB (Default) 0110 = Shift 6LSB; 0111 = Shift 7LSB; 1000 = Shift 8LSB; 1001 = Shift 9LSB; 1010 = Shift 10LSB
0x3F	VDDA	ALCHVID[7:0]	R/W	48h	VDDA Latch VID Register, Default = 48h = 1.1V
0x44	VDDA	AVM0[7:0]	R/W	00h	VIMONA > Level 0 => LCS0 VIMONA < Level 0 => LCS1 (lowest current state) (For 2-phase operation of VDDA) Bit[1:0] : Don't care AVM0 = (Bit[7:2]/64) x2.56 AVM0 setting is defined as the ratio to IMON voltage to 2.56V
0x45	VDDA	ATM[7:0]	RO	00h	VDDA SMBus Thermal Monitor Value Reading. This register stores the value of A/D conversion for TSENA pin
0x46	VDDA	AProtect_Ind [6:0]	RO	00h	VDDA protection indicator, indicating which protection is triggered Bit[7] : Don't care Bit[6] : OVP Indicator "0" = Not Active, "1" = Active Bit[5] : UVP Indicator "0" = Not Active, "1" = Active Bit[4] : OCP Indicator "0" = Not Active, "1" = Active Bit[3] : Per Phase OCP Indicator "0" = Not Active, "1" = Active Bit[2:1]: Don't care Bit[0]: "0" = PH2, "1" = PH1 Report value of Bit[0] is valid only when Bit[3]=1

Reg. Addr.	Focus Rail	Reg. Name	Access	Default	Description
0x47	VDD	VRSD[7:4] VRSD Hys [3:0]	R/W	70h	VDD PWM controller OTP shutdown threshold setting Bit[7:4]: 16 steps, 2°C/step VR_SHDN = 111°C + (Bit[7:4])x2, temp range from 111°C to 141°C, default = 125°C VR_SHDN Hysteresis Setting Bit[3:0]: 16 steps , 2°C/step VR_SHDN Hys = (Bit[3:0])x2
0x48	VDDA	AVRSD[7:4] AVRSD Hys [3:0]	R/W	70h	VDD PWM controller OTP shutdown threshold setting Bit[7:4]: 16 steps, 2°C/step VR_SHDN = 111°C + (Bit[7:4])x2, temp range from 111°C to 141°C, default = 125°C VR_SHDN Hysteresis Setting Bit[3:0]: 16 steps , 2°C/step VR_SHDN Hys = (Bit[3:0])x2
0x4A	shared	CHIP ID	RO	29h	

Absolute Maximum Rating

(Note 1)

Supply Input Voltage VCC5 to GND ---------- -0.3V to +6V
VINSEN ---------- -0.3V to +30V
Other Pins to GND ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN6x6 - 52L θ_{JA} ---------- 35°C/W
VQFN6x6 - 52L θ_{JC} ---------- 3°C/W
Power Dissipation, P_D @ T_A = 25°C
VQFN6x6 - 52L ---------- 2.86W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage VCC5 ---------- 4.5V to 5.5V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(VCC5 = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
VCC5 POR Threshold	POR_{VCC5}	VCC5 rising	4.1	4.3	4.5	V
VCC5 POR Hysteresis	$HYS_{VCC5POR}$		--	0.3	--	V
Supply Current	I_{VCC5}	EN = 5V, VDD and VDDA VID = 0V, PWM no switching	--	10	--	mA
Shutdown Current	I_{VCC5_SHDN}	EN = 0V	--	60	--	uA
VIN Sense						
VINSEN POR Threshold	POR_{VINSEN_r}	VINSEN rising	--	6	--	V
VINSEN POR Threshold	POR_{VINSEN_f}	VINSEN falling	--	4.5	--	V
Input Current	I_{VINSEN}	EN = 5V, VINSEN = 12V	--	30	--	uA
EN Input						
Input Low	V_{IL}		--	--	0.8	V
Input High	V_{IH}		2	--	--	V
Pull-Low Current	I_{EN_PL}		1	2	3	uA
SVI2 Bus Timing Parameters (Guaranteed by design)						
SVC Period	T_{PERIOD}		47.6	--	--	ns
SVC Frequency	F_{SVC}		0.1	--	21	MHz
SVC High Time	T_{HIGH}		20	--	--	ns
SVC Low Time	T_{LOW}		30	--	--	ns
SVD,SVT Setup Time to SVC rising edge	T_{Setup}		5	--	--	ns
SVD,SVT Hold Time from SVC falling edge	T_{Hold}		5	--	--	ns
SVD,SVT Start Time to SVC falling edge	T_{START}		15	--	--	ns
SVD,SVT Stop Time from SVC rising edge	T_{STOP}		5	--	--	ns
SVC, SVD, SVT, Fall Time	T_{FALL}	V_{OH_DC} to V_{OL_DC}	--	--	1	ns
SVC, SVD, SVT, Rise Time	T_{RISE}	V_{OL_DC} to V_{OH_DC}	--	--	1	ns

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
SVI2						
SVC,SVD,SVT and PWROK input Low Voltage	V_{IL_DC}		0	--	0.35* VDDIO	V
SVC,SVD,SVT and PWROK input High Voltage	V_{IH_DC}		0.7* VDDIO	--	VDDIO	V
SVC,SVD,SVT and PWROK Hysteresis Voltage	V_{HYST}		0.1* VDDIO	--	--	V
SVC,SVD,SVT Low Level Output Voltage	V_{OL}		0	--	0.2	V
SVC,SVD,SVT High Level Output Voltage	V_{OH}		VDDIO -0.2	--	VDDIO	V
SVC,SVD,SVT Output Current	I_{OH}	when driving V_{OH}	4	--	--	mA
SVC,SVD,SVT, PWROK Input Leakage Current	I_L		-100	--	100	uA
SVD High Z Output Leakage Current	I_{OZ}		-100	--	100	uA
SVC,SVD,SVT Input Capacitances	C_{IN}	Guaranteed by design	--	--	5	pF
Telemetry and ADC						
ADC Accuracy		0.8V to 1.2V	-1	--	1	LSB
		>1.2V or < 0.8V	-2	--	2	
DAC Voltage Accuracy (DAC, DACA)						
DAC Voltage Accuracy	V_{DAC}	0.5V < VID ≤ 0.8V	-15	--	15	mV
		0.8V < VID ≤ 1.0V	-10	--	10	mV
		1.0V < VID ≤ 1.55V	-1	--	1	%
Slew Rate (DAC, DACA)						
Slew Rate	SR		10	12	--	mV/ us
Error Amplifier						
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Trans-Conductance	GM		--	2020	--	uA/V
Gain Bandwidth Product	$G_{BW(EA)}$	Guaranteed by Design	--	10	--	MHz
PWM On-Time Setting						
PWM On Time	T_{ON}	VINSEN = 12V, VID = 1.2V, R_{TONSET} = 50kΩ, Fsw=200kHz	--	500	--	ns
Minimum Off-Time	T_{OFF_MIN}	Single phase operation	--	300	--	ns
Current Sense Amplifier for Total Current Summing						
Offset Voltage	$V_{OS(CSA)}$		-1	--	1	mV
Input Bias Current	$I_{BC(CSA)}$	V_{CSPx} = 1.2V, guaranteed by design	-10	--	10	nA

Electrical Characteristics

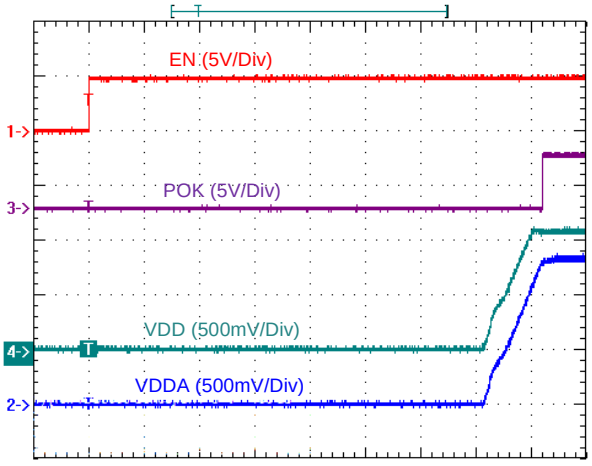
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Current Sense Amplifier for Total Current Summing (cont'd)						
Maximum Sourcing Current	I_{MAXSRC}		100	--	--	uA
Gain Bandwidth Product	$G_{BW(CSA)}$	Guaranteed by Design	--	10	--	MHz
Current Sense Amplifier for Phase Current Balance						
Offset Voltage	$V_{OS(CSA)}$		-1	--	1	mV
Input Bias Current	$I_{BC(CSA)}$	V_{CSPx} = 1.2V, guaranteed by design	-10	--	10	nA
Maximum Sourcing Current	I_{MAXSRC}		100	--	--	uA
Gain Bandwidth Product	$G_{BW(CSA)}$	Guaranteed by Design	--	10	--	MHz
PWM Output						
Output Low Voltage	$V_{OL(PWM)}$	I_{SINK} = 4mA	--	--	0.2	V
Output High Voltage	$V_{OH(PWM)}$	I_{SOURCE} = 4mA	4.7	--	--	V
High Impedance State Leakage	I_{PWM_leak0}	V_{PWM} = 0V	-1	--	0	uA
	I_{PWM_leak1}	V_{PWM} = 5V	0	--	1	uA
Current Monitoring for Droop						
Current Mirror Ratio for VDD		I_{EAP} to I_{CSN} ratio	95	100	105	%
Current Mirror Ratio for VDDA		I_{EAPA} to I_{CSNA} ratio	95	100	105	%
VRHOT#, POK						
Output Low Voltage	V_{OL}	I_{SINK} = 4mA	--	--	0.2	V
Output Leakage Current	I_L	Pull up to 5V	--	--	1	uA
Over Current Protection						
Current Mirror Ratio for VDD		I_{MON} to I_{CSN} ratio	95	100	105	%
Current Mirror Ratio for VDDA		I_{MONA} to I_{CSNA} ratio	95	100	105	%
Total Current OCP Threshold	V_{IMON_OCP}		2.54	2.56	2.58	V
Total Current OCP Delay Time	T_{OCP1_DELAY}		--	20	--	us
Over Current Protection (cont'd)						
Per-Phase OCP Threshold	I_{OCP2}	Measure I_{CSNX} current	--	100	--	uA
Per-Phase OCP Delay Time	T_{OCP2_DELAY}		--	6	--	us
Under Voltage Protection						
UVP Threshold	V_{UVP}	V_{EAP} - V_{FB}; V_{EAPA} - V_{FBA}	300	325	350	mV
UVP Delay Time	T_{UVP}		--	8	--	us
Over Voltage Protection						
OVP Threshold	V_{OVP}	V_{FB} - V_{EAP}; V_{FBA} - V_{EAPA}	300	325	350	mV
OVP Delay Time	T_{OVP}		--	6	--	us

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Thermal Shutdown Protection						
OTP Threshold	T_{OTP}		--	160	--	°C
Thermal Monitoring						
VRHOT# Assert Threshold	V_{TSEN_R}	Temperature ADC result = 106°C, measure TSEN/TSENA voltage	--	4.383	--	V
VRHOT# De-Assert Threshold	V_{TSEN_F}	Temperature ADC result = 102°C, measure TSEN/TSENA voltage	--	4.326	--	V

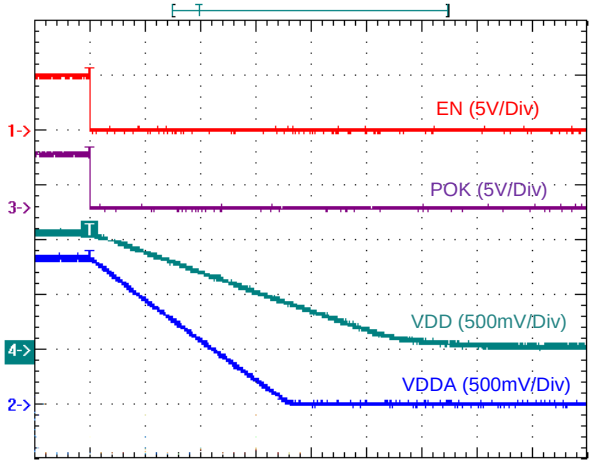
Typical Operation Characteristics

Power On from EN



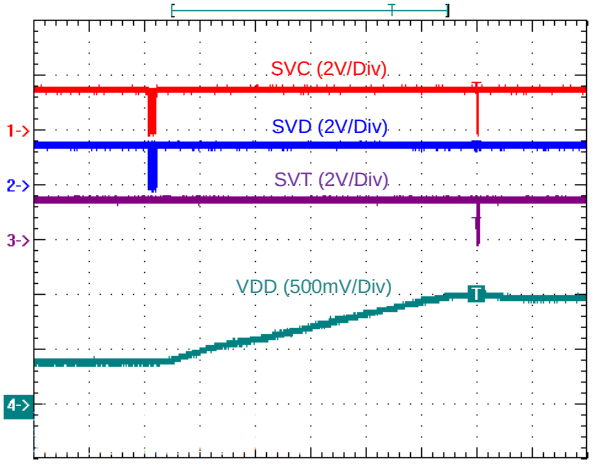
Time：100us/Div
V_{IN} = 12V, no load

Power Off from EN



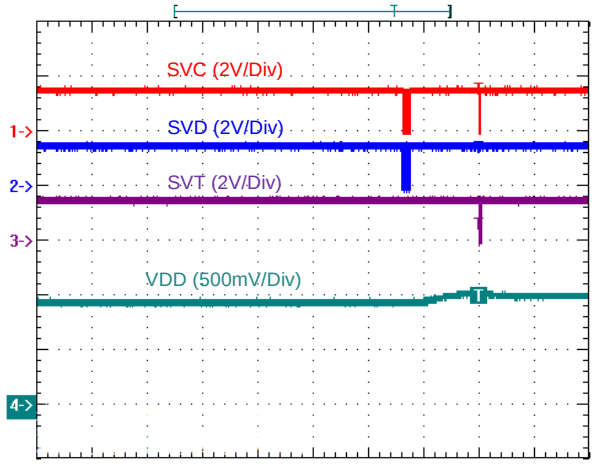
Time：1ms/Div
V_{IN} = 12V, I_{OUT} = 1A

VDD VR Dynamic VID Up



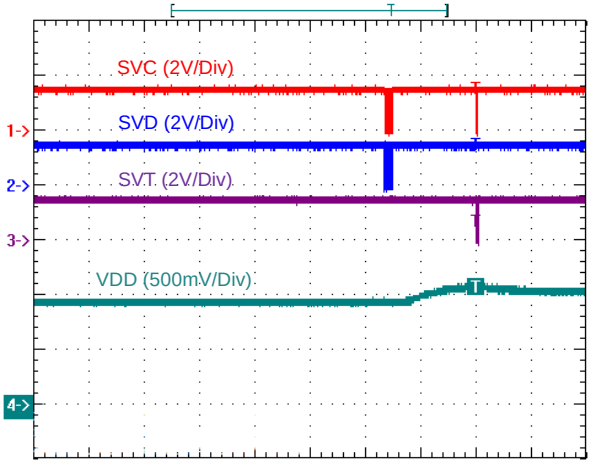
Time：10us/Div
VID = 0.4V to 1V, I_{LOAD} = 9A

VDD VR Dynamic VID Up



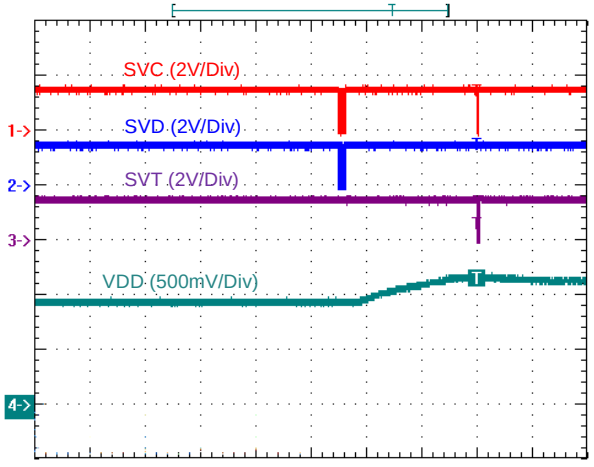
Time：10us/Div
VID = 1V to 1.06875V, I_{LOAD} = 45A

VDD VR Dynamic VID Up



Time：10us/Div
VID = 1V to 1.1V, I_{LOAD} = 45A

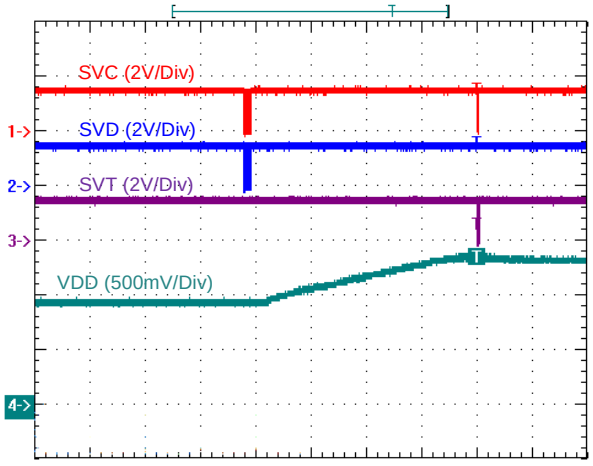
VDD VR Dynamic VID Up



Time：10us/Div
VID = 1V to 1.2V, I_{LOAD} = 45A

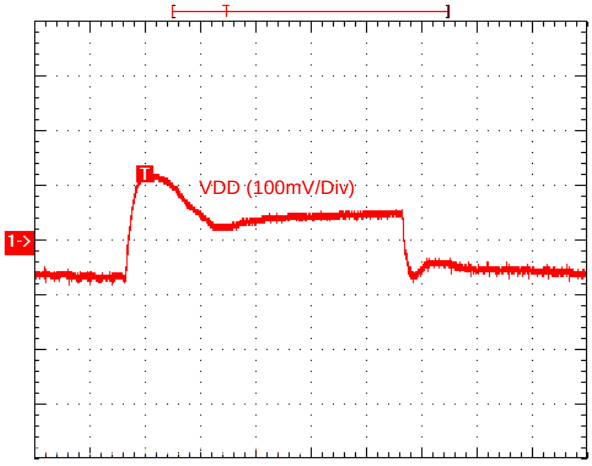
Typical Operation Characteristics

VDD VR Dynamic VID Up



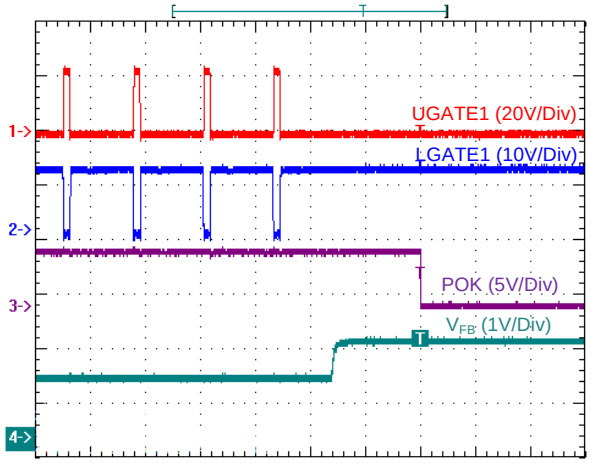
Time：10us/Div
VID = 1V to 1.4V, I_{LOAD} = 45A

VDD VR Load Transient



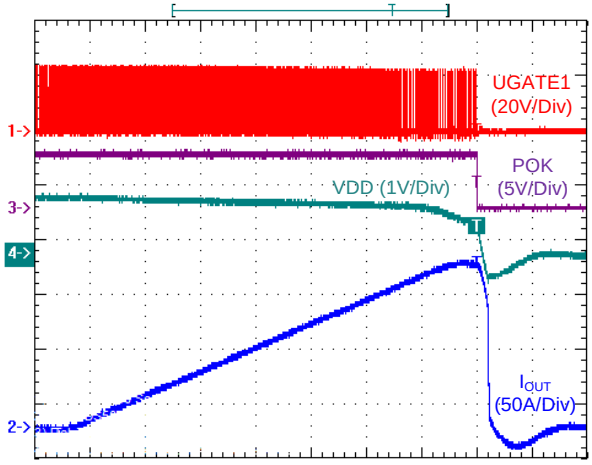
Time：10us/Div
F_{LOAD} = 10kHz, VDD = 1V, I_{LOAD} = 35A ~ 120A

VDD VR OVP



Time：4us/Div

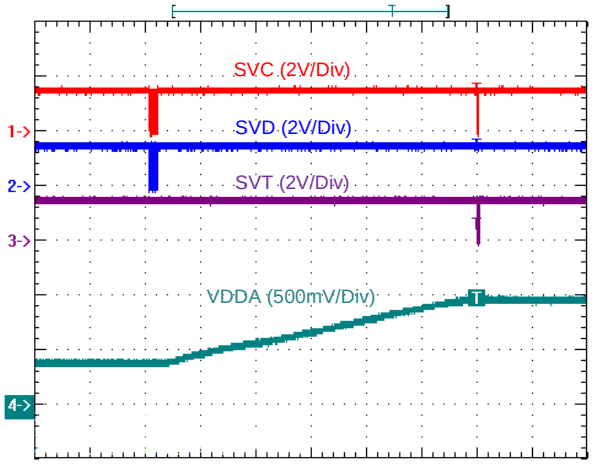
VDD VR OCP



Time：200us/Div

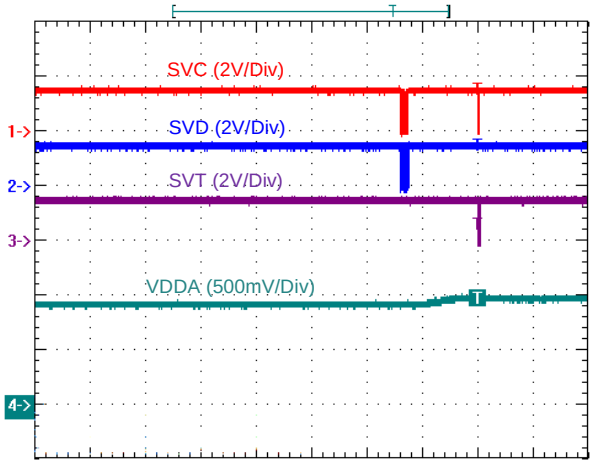
Typical Operation Characteristics

VDDA VR Dynamic VID Up



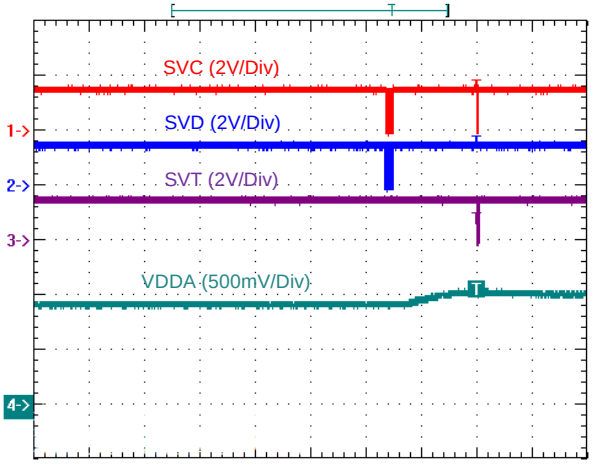
Time：10us/Div
VID = 0.4V to 1V, I_{LOAD} = 4.1A

VDDA VR Dynamic VID Up



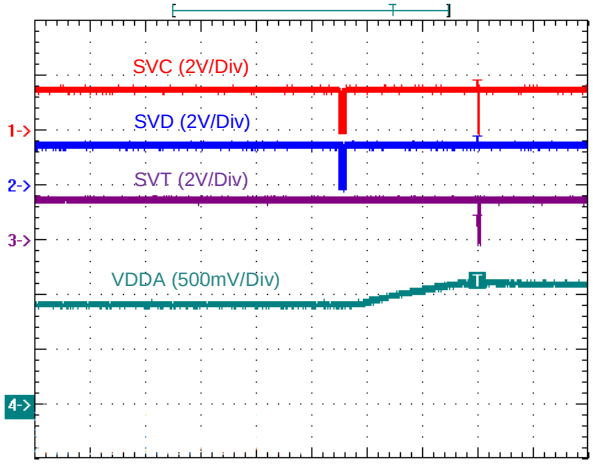
Time：10us/Div
VID = 1V to 1.06875V, I_{LOAD} = 20.5A

VDDA VR Dynamic VID Up



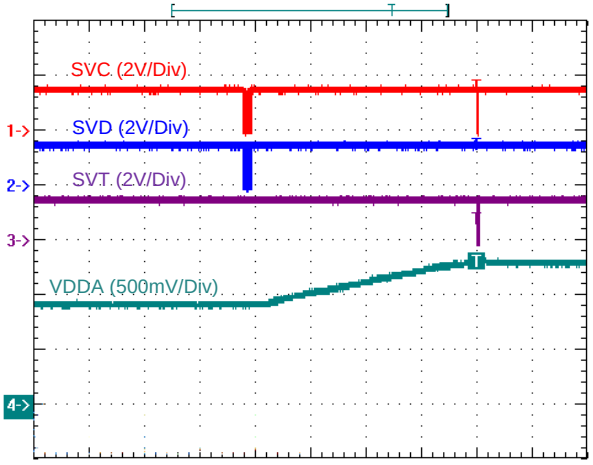
Time：10us/Div
VID = 1V to 1.1V, I_{LOAD} = 20.5A

VDDA VR Dynamic VID Up



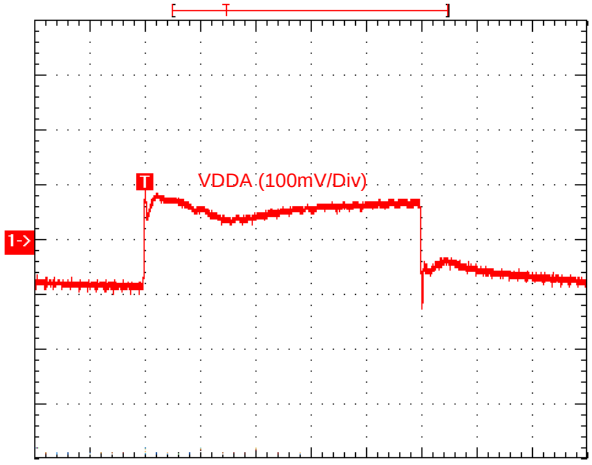
Time：10us/Div
VID = 1V to 1.2V, I_{LOAD} = 20.5A

VDDA VR Dynamic VID Up



Time：10us/Div
VID = 1V to 1.4V, I_{LOAD} = 20.5A

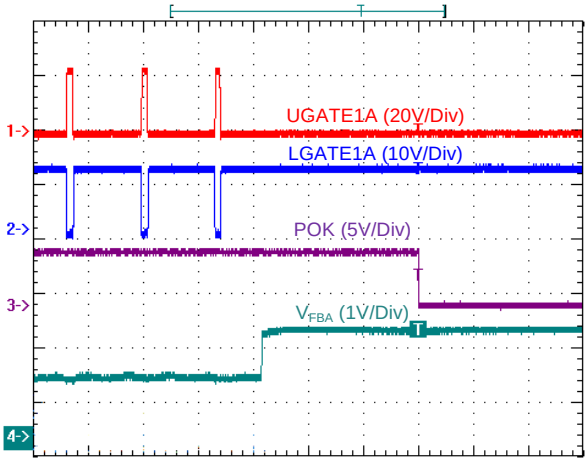
VDDA VR Load Transient



Time：10us/Div
F_{LOAD} = 10kHz, VDDA = 1V, I_{LOAD} = 20A ~ 60A

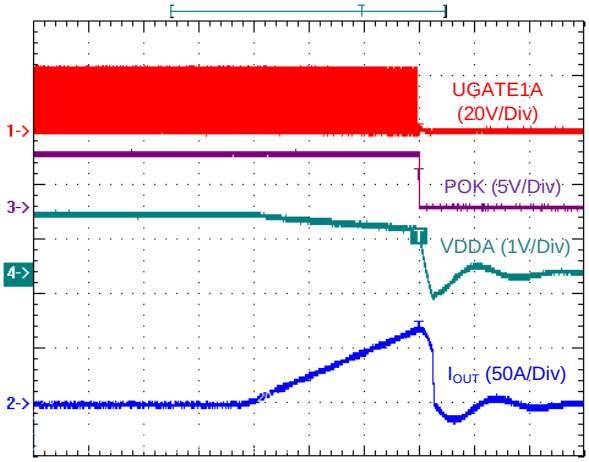
Typical Operation Characteristics

VDDA VR OVP



Time：4us/Div

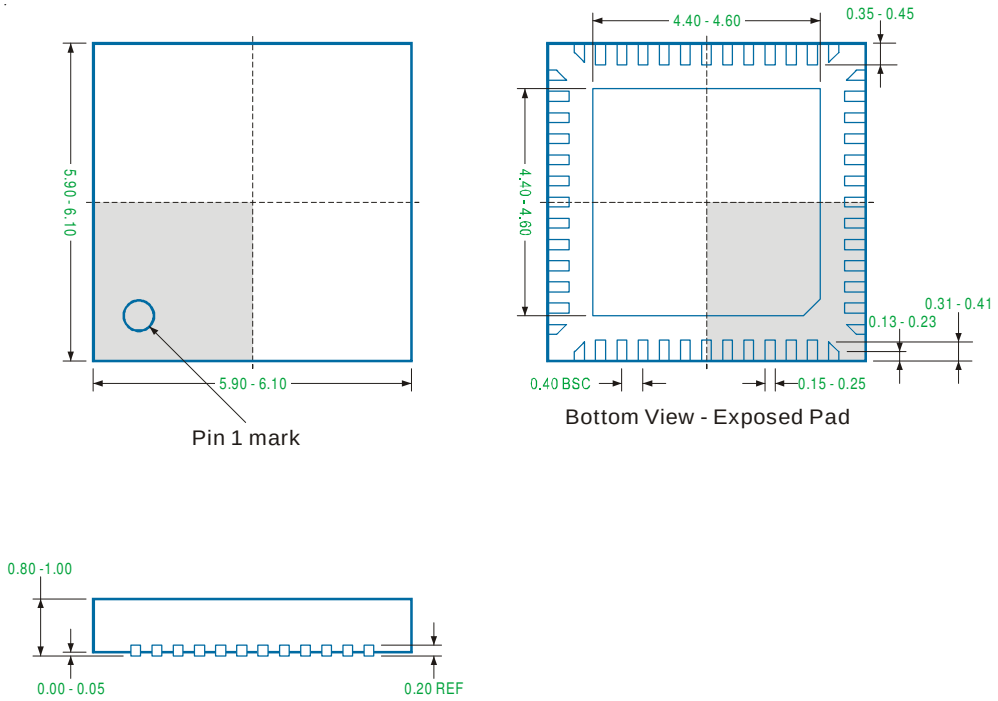
VDDA VR OCP



Time：200us/Div

Package Information

VQFN6x6 - 52L Package



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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